

Compal Confidential

EA50_KV M/B Schematics Document

AMD Kaveri(FP3) + Bolton(M3)

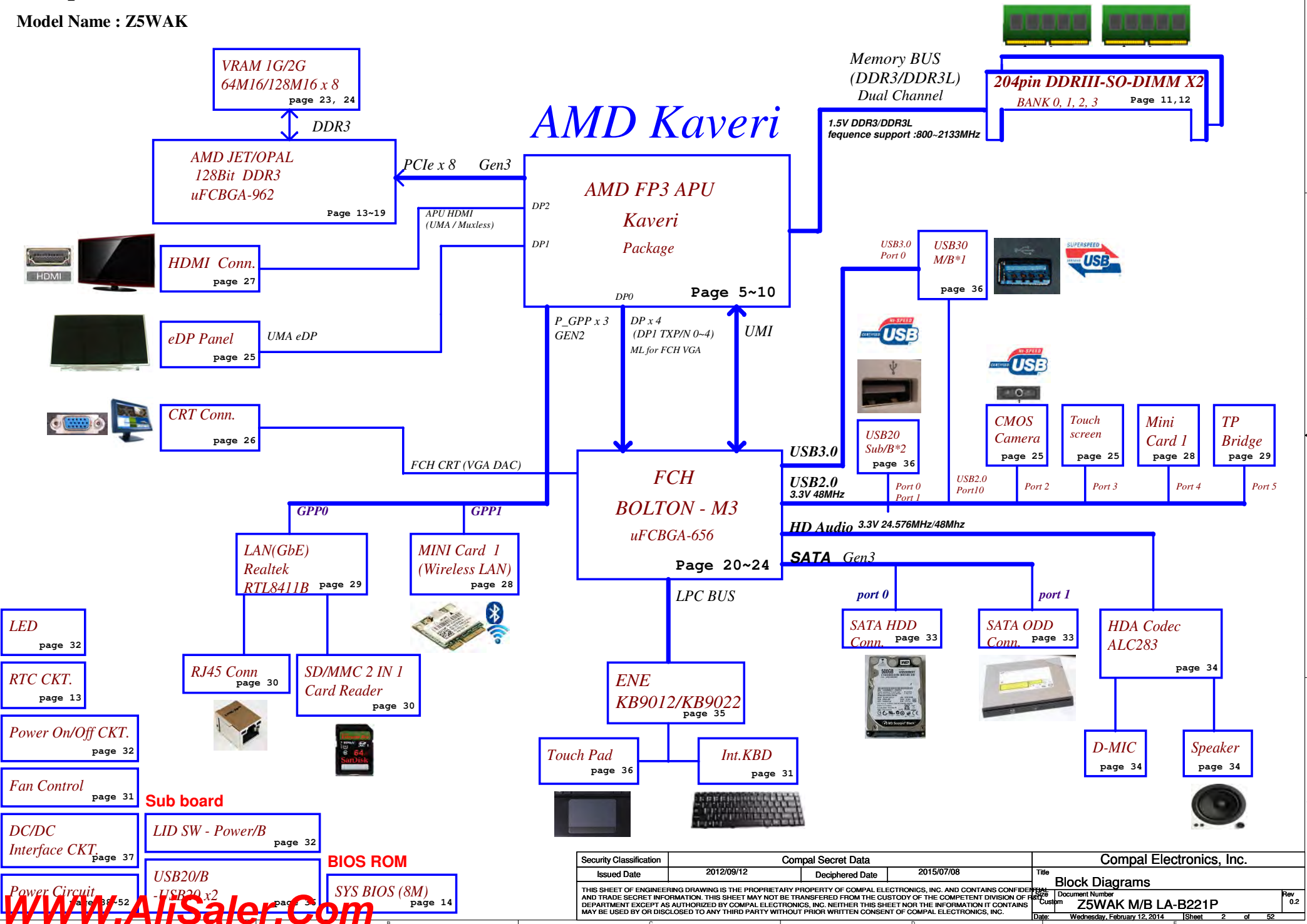
AMD OPAL / JET

2013-02-11

REV : 0.3

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Issued Date	2012/09/12	Deciphered Date	2015/07/08	Title	
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Model Name : Z5WAK



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Issued Date	2012/09/12	Deciphered Date	2015/07/08	Title	Block Diagrams
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Voltage Rails

Power Plane	Description	S0	S3	S4	S5
VIN	Adapter power supply (19V)	ON	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON	ON
+CPU_CORE	Core voltage for APU	ON	OFF	OFF	OFF
+CPU_CORE_NB	Voltage for VDDNB	ON	OFF	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	DIS	OFF	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	DIS	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+0.95VSDGPU	1.0V switched power rail for VGA	DIS	OFF	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	AC/DC	AC/DC
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail for APU	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5VSDGPU	1.5V switched power rail for VGA	DIS	OFF	OFF	OFF
+1.8VSDGPU	1.8V switched power rail for VGA	DIS	OFF	OFF	OFF
+1.8VS	1.8VS for CPU_VDDA	ON	OFF	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	WOL	WOL
+3VS_WLAN	3.3V power rail for WLAN	ON	IOAC	IOAC	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON	ON

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X	16H	SB-TSI (APU)	1001 100X	96H
			VGA Internal Thermal		

FCH SM Bus 0 address

FCH SM Bus 1 address

Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000Xb	A0H			
DDR DIMM2	1010 001Xb	A2H			
MINI CARD					

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
0	0		0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V		0xE7 - 0xFF



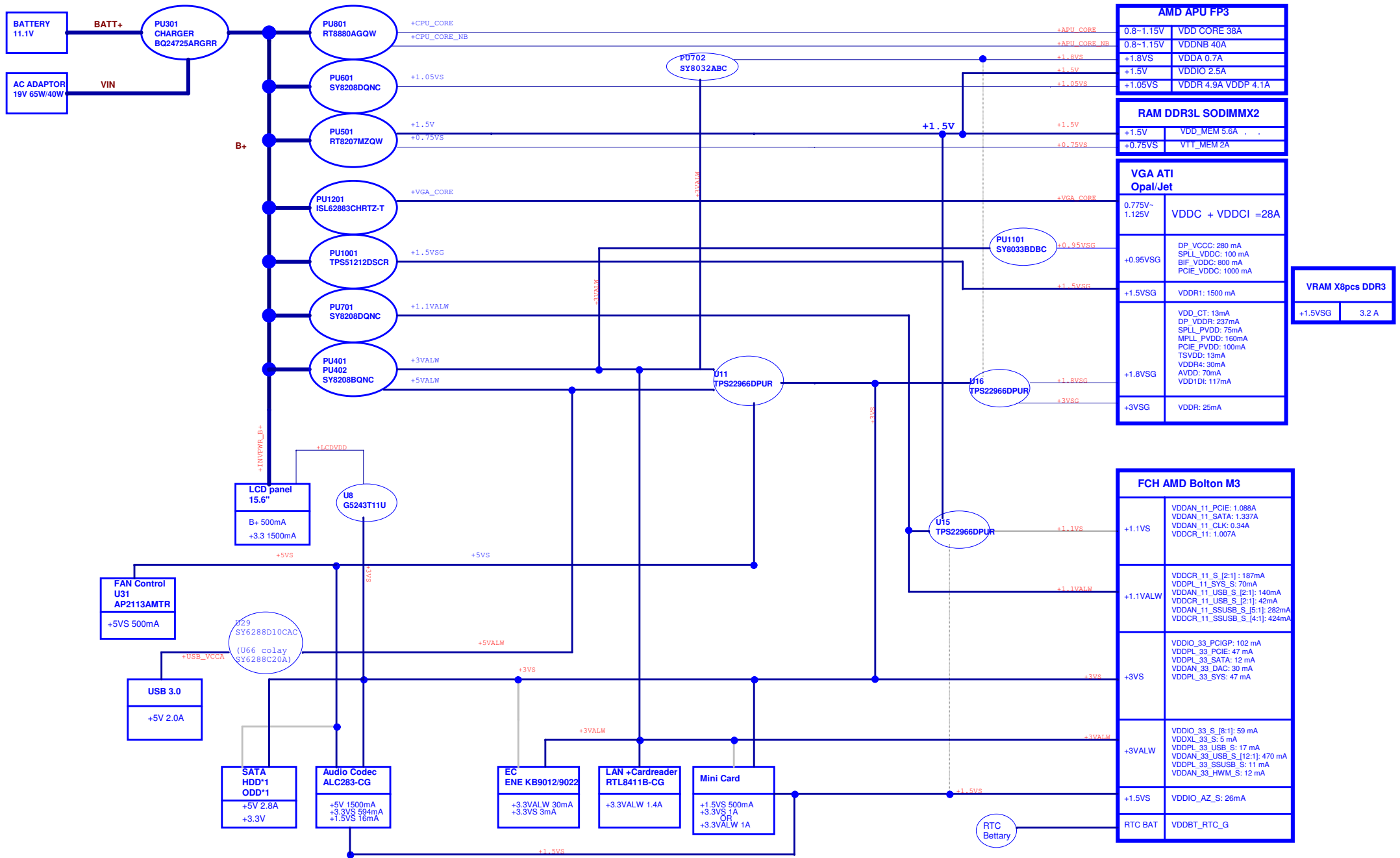
BOARD ID Table

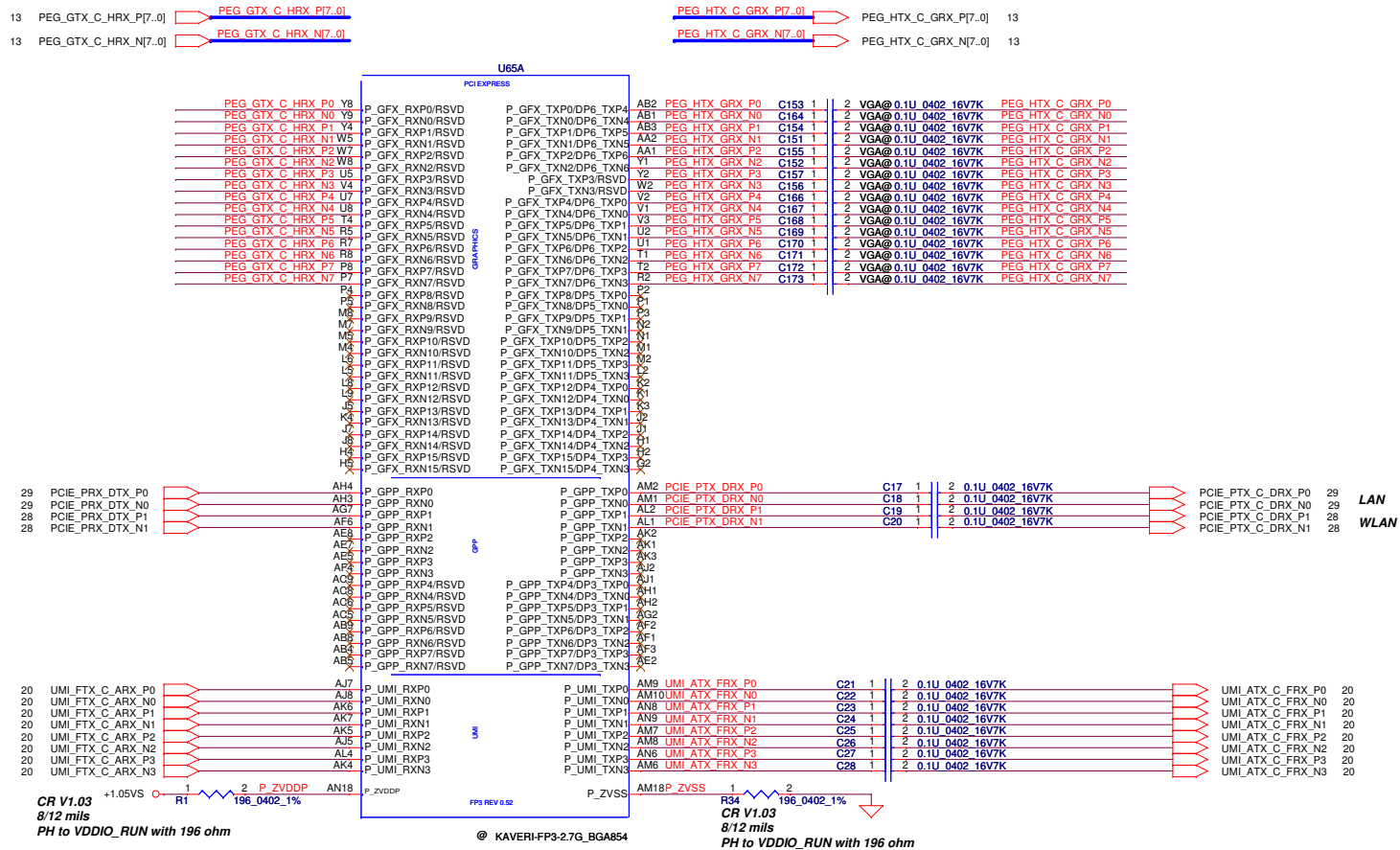
Board ID	PCB Revision
0	EVT
1	DVT
2	
3	
4	
5	
6	
7	

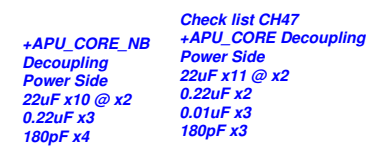
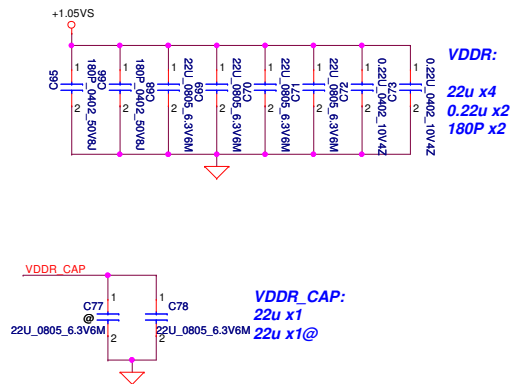
BOM Option Table

BOM Structure	Description
9022@	Use EC 9022
9012@	Use EC 9012
UMA@	Display output from APU (UMA only)
VGA@	Use VGA (PX or DIS only)
AL@	Use Auto load EC code function
AC@	Support AC Function
NOAC@	No Support AC Function
TPM@	Support D TPM function
CONN@	Connector (Control by ME)
HDT@	Debug Connector
EMC@	EMC Component
XEMC@	Reservec for EMC
TPSM@	Use APU SMBus for T/P
TPBRI@	Use USB to I2C IC for T/P
USBTP@	Use USB T/P
MOS@	Use MOSART solution USB to I2C TP
X76@	VRAM ID Table (Load By X76J)
128@	VRAM x 8pcs
OPAL@	ATI OPAL VGA CONTROLLER
JET@	ATI JET VGA CONTROLLER
BL@	BACK LIGHT CIRCUIT
@	Unpop
X76@	VRAM type select

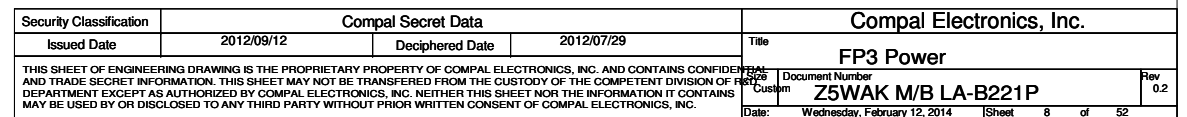
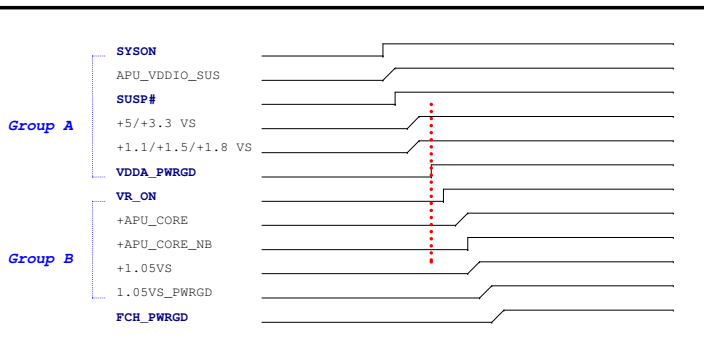
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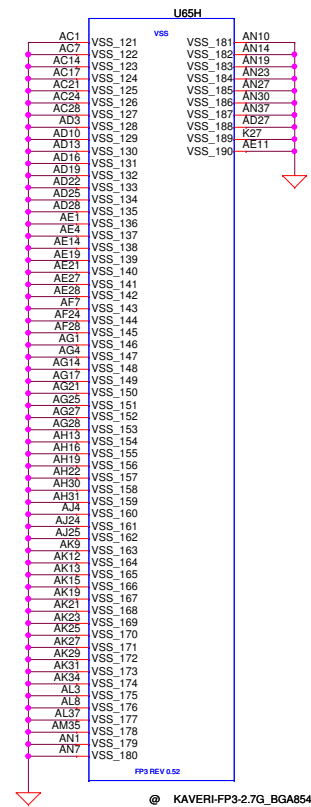
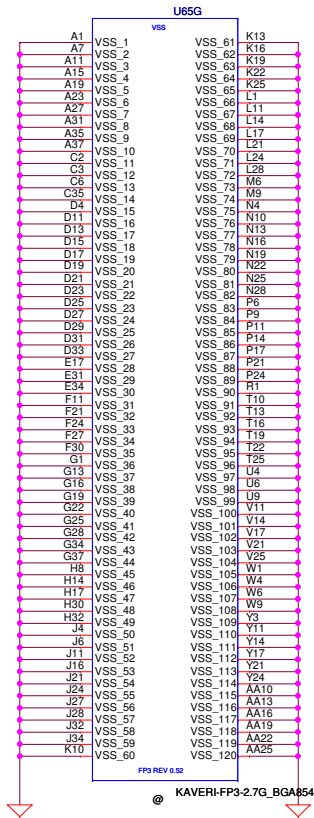






Power Name	Consumption
VDD +APU_CORE	38A
VDDNB +APU_CORE_NB	40A
VDDIO +1.5V	2.5A
VDDP / VDDR +1.05VS	4.0A / 3.9A
VDDA +1.8VS	0.7A





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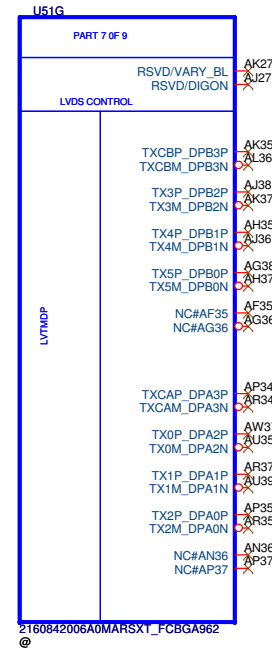
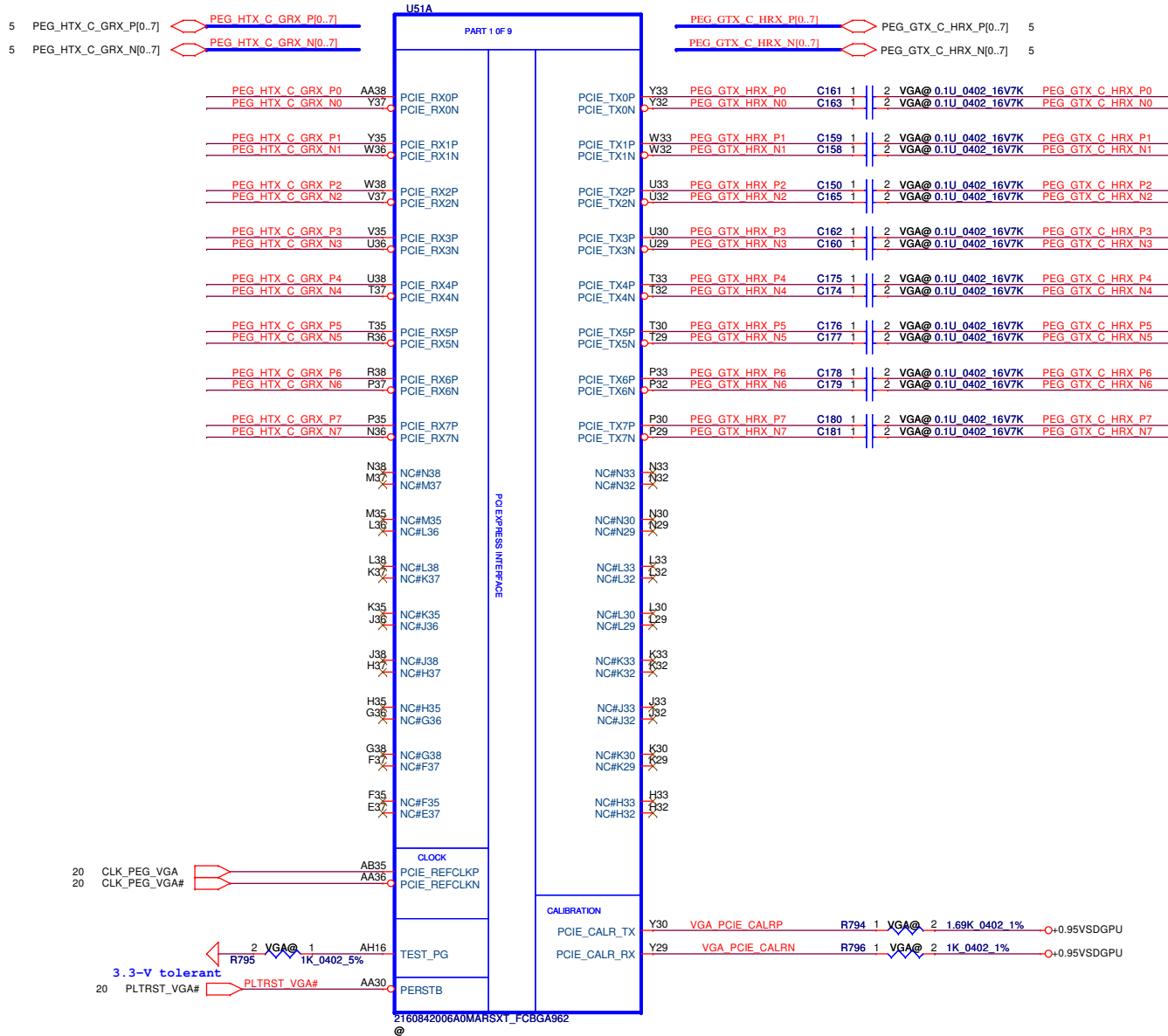
Panel ENBKL


Panel ENVDD

Panel PWM

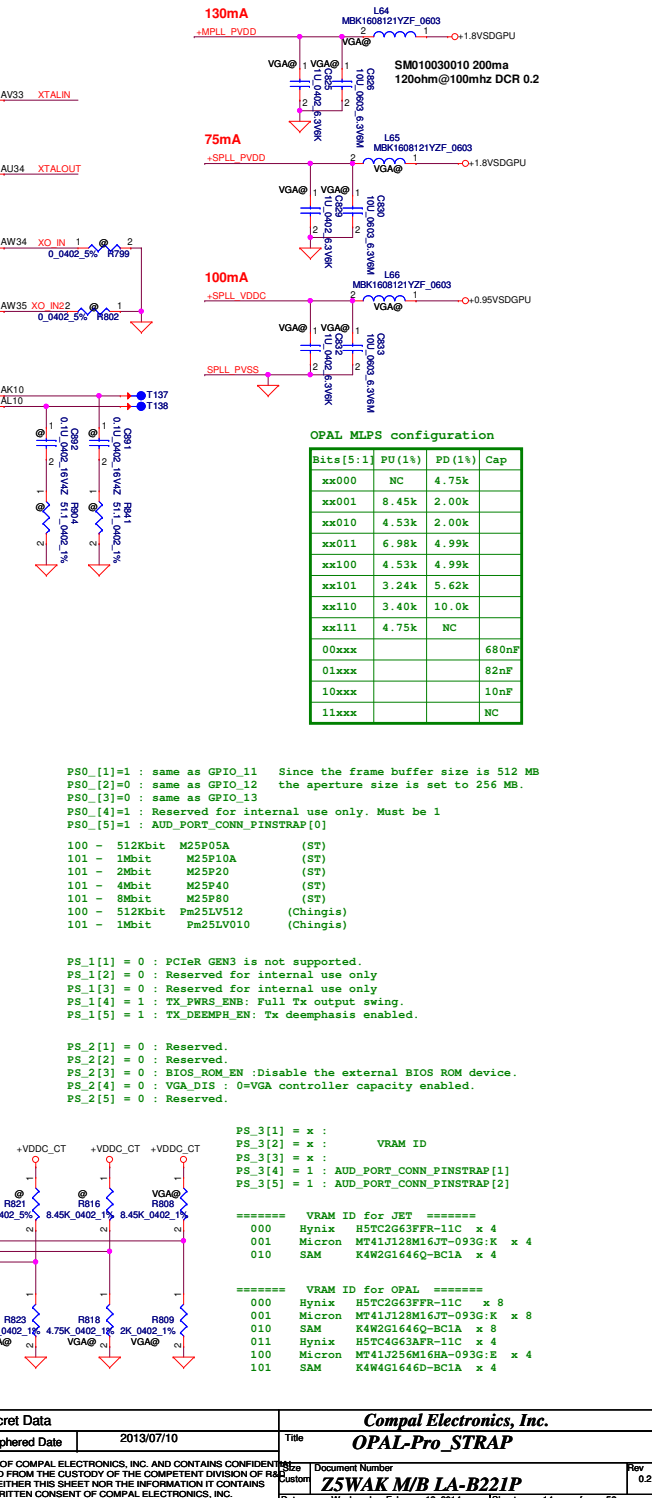
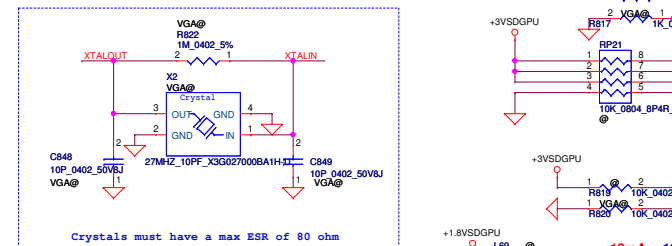
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Issued Date	2011/07/08	Deciphered Date	2015/07/08	AMD FS1R2 Singal Level Shifter	
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GFX PCIE LANE REVERSAL



U51

OPAL XT M2 FCBGA
OPAL@
SA000078V20
CHANGE TO R
02/11

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Bits{5:1}	PU (1%)	PD (1%)	Cap
xx000	NC	4.75k	
xx001	8.45k	2.00k	
xx010	4.53k	2.00k	
xx011	6.98k	4.99k	
xx100	4.53k	4.99k	
xx101	3.24k	5.62k	
xx110	3.40k	10.0k	
xx111	4.75k	NC	
00xxx			680nF
01xxx			82nF
10xxx			10nF
11xxx			NC

```

PS0_1[1] = 1 : same as GPIO_11      Since the frame buffer size is 512 MB
PS0_2[2] = 0 : same as GPIO_12      the aperture size is set to 256 MB.
PS0_3[3] = 0 : same as GPIO_13
PS0_4[4] = 0 : Reserved for internal use only. Must be 1
PS0_5[5] = 1 : AUD_PORT_CONN_PINSTRAP[0]

100 - 512Kbit M25P05A      (ST)
101 - 1MbIt M25P10A      (ST)
101 - 2MbIt M25P20      (ST)
101 - 4MbIt M25P40      (ST)
101 - 8MbIt M25P80      (ST)
100 - 512Kbit Pm25LV512 (Chingis)
101 - 1MbIt Pm25LV010 (Chingis)

PS_1[1] = 0 : PCIeR GEN3 is not supported.
PS_2[2] = 0 : Reserved for internal use only
PS_3[3] = 0 : Reserved for internal use only
PS_4[4] = 1 : TX_PWRS_ENB: Full Tx output swing.
PS_5[5] = 1 : TX_DEEMPH_EN: Tx deemphasis enabled.

PS_2[1] = 0 : Reserved.
PS_2[2] = 0 : Reserved.
PS_2[3] = 0 : BIOS_ROM_EN:Disable the external BIOS ROM device.
PS_2[4] = 0 : VGA_DIS : 0=VGA controller capacity enabled.
PS_2[5] = 0 :

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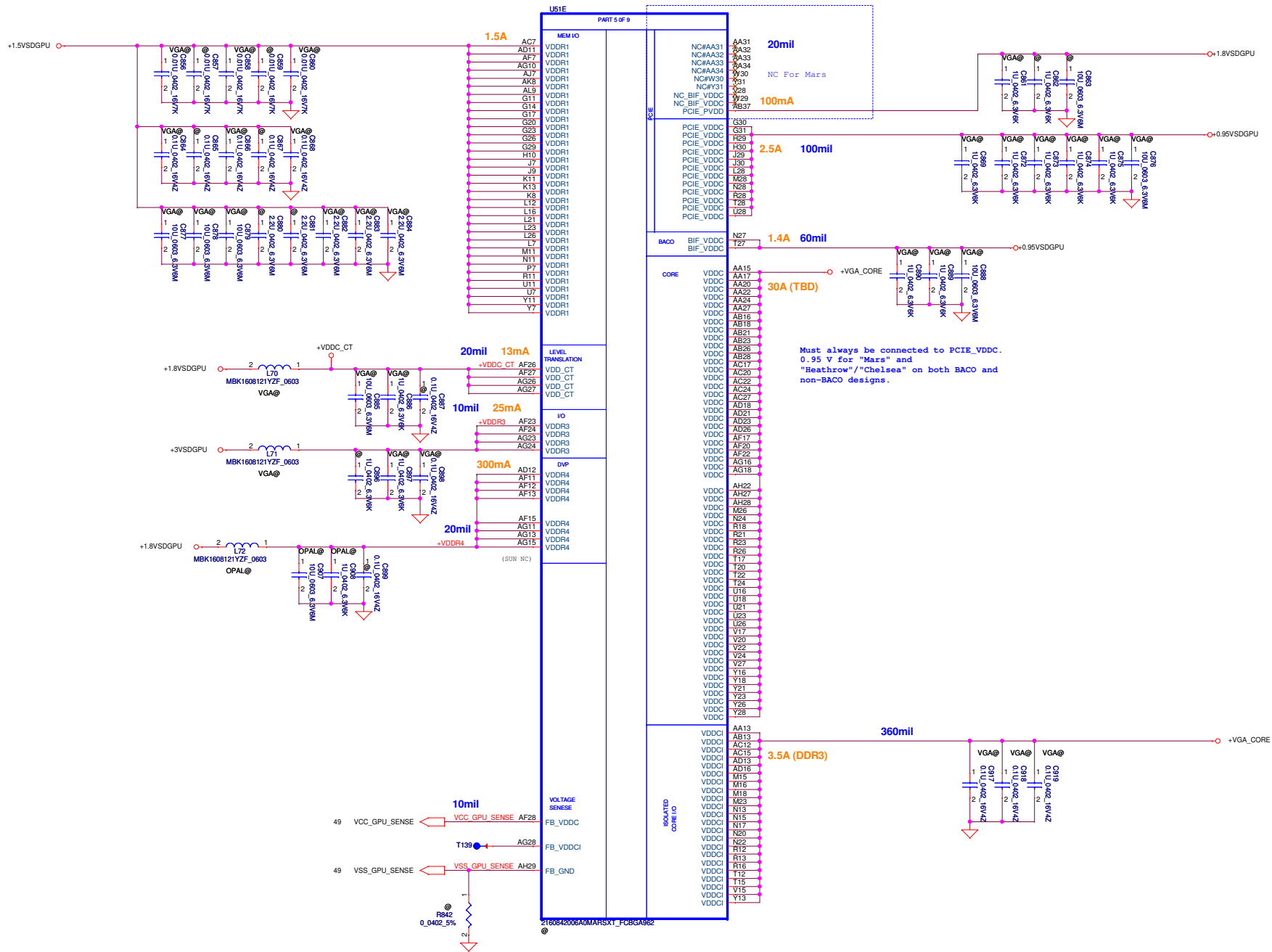
PS_3[1] = x :
PS_3[2] = x :          VRAM ID
PS_3[3] = x :
PS_3[4] = 1 :          AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] = 1 :          AUD_PORT_CONN_PINSTRAP[2]

===== VRAM ID for JET =====
000 Hynix H5TC26G3F3FR-11C x 4
001 Micron MT41J28M16J7T-093G-K x 4
010 SAM K4W2016460-BC1A x 8

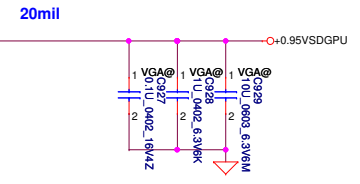
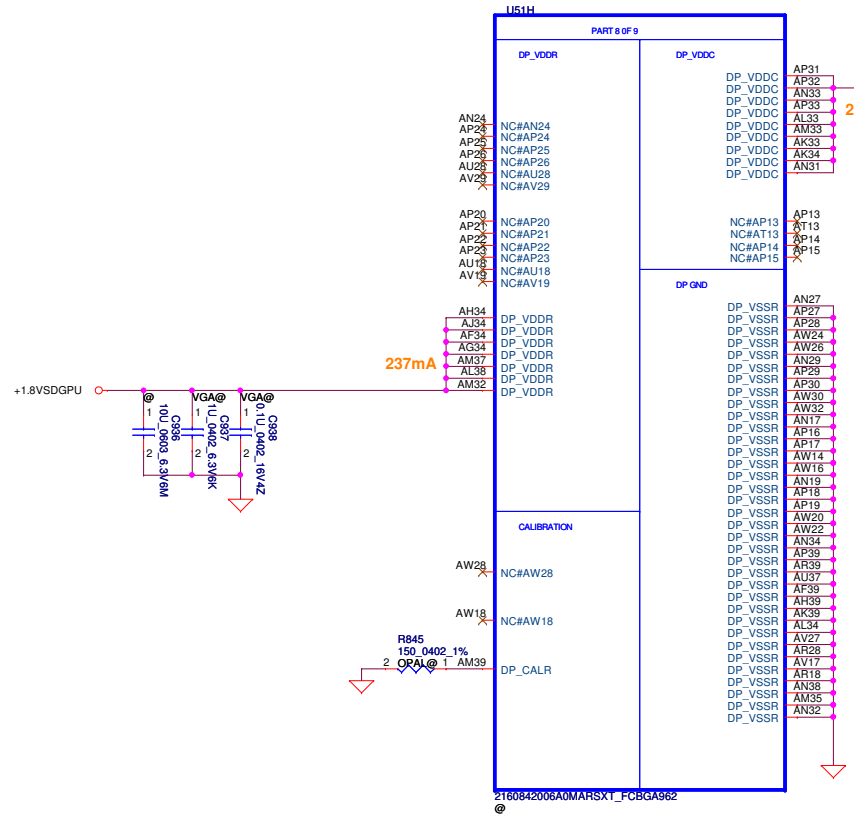
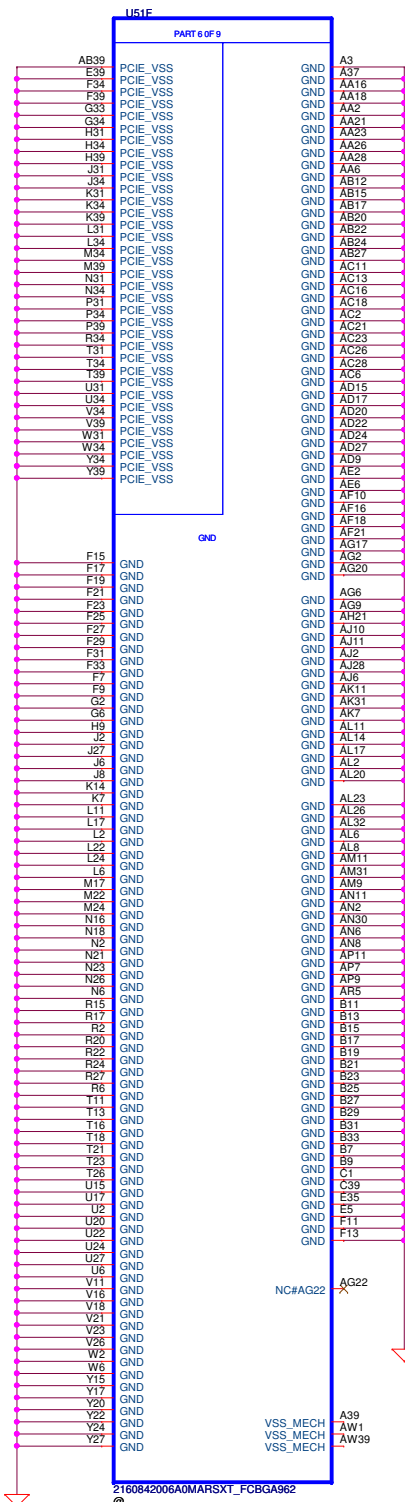
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001 Micron MT41J28M16J7T-093G-K x 8
010 SAM K4W2016460-BC1A x 8
111 Hynix H5TC46G3AFR-11C x 4
100 Micron MT41J28M16J7T-093G-K x 4
101 SAM K4W4G16460-BC1A x 4

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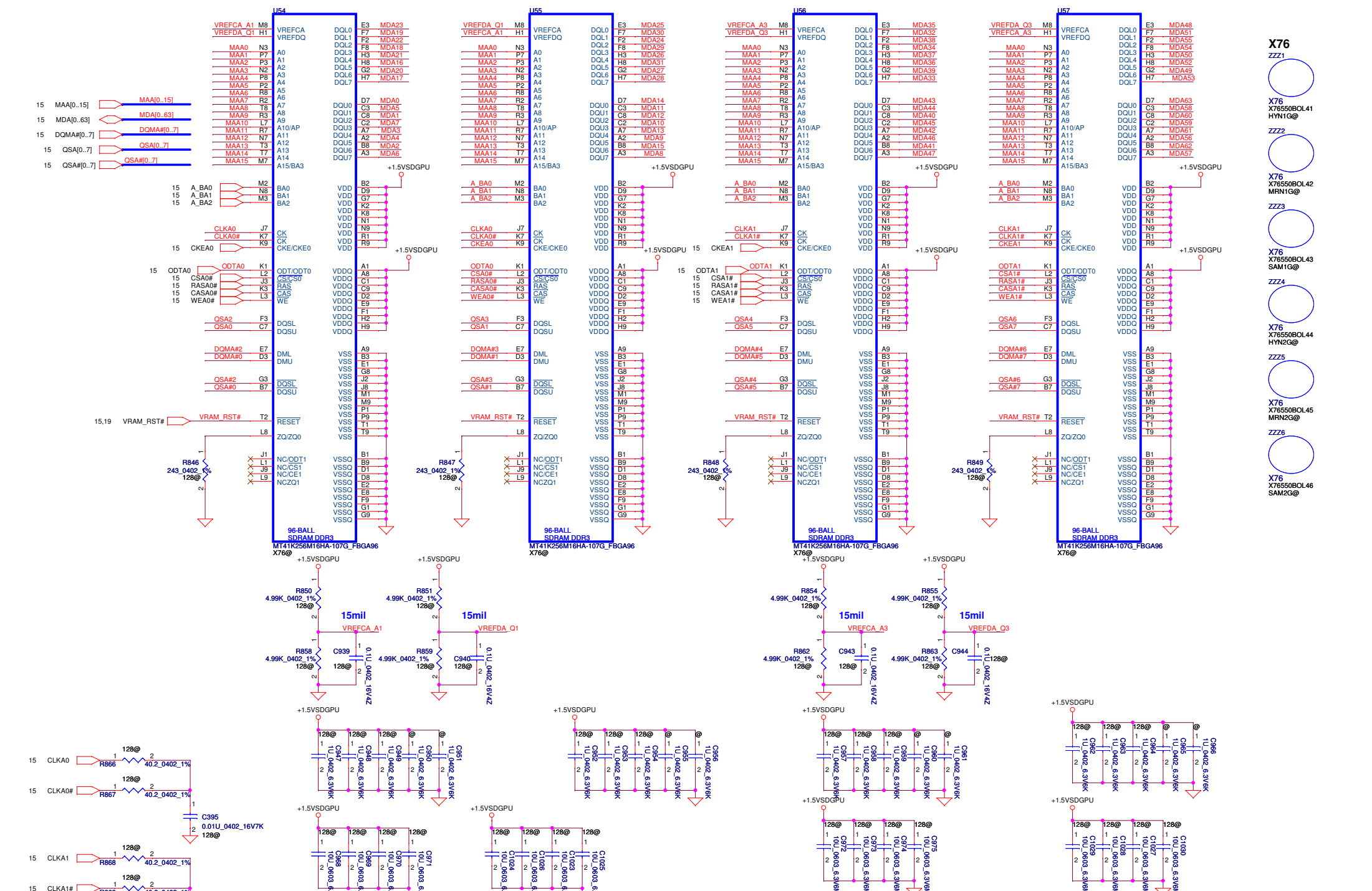
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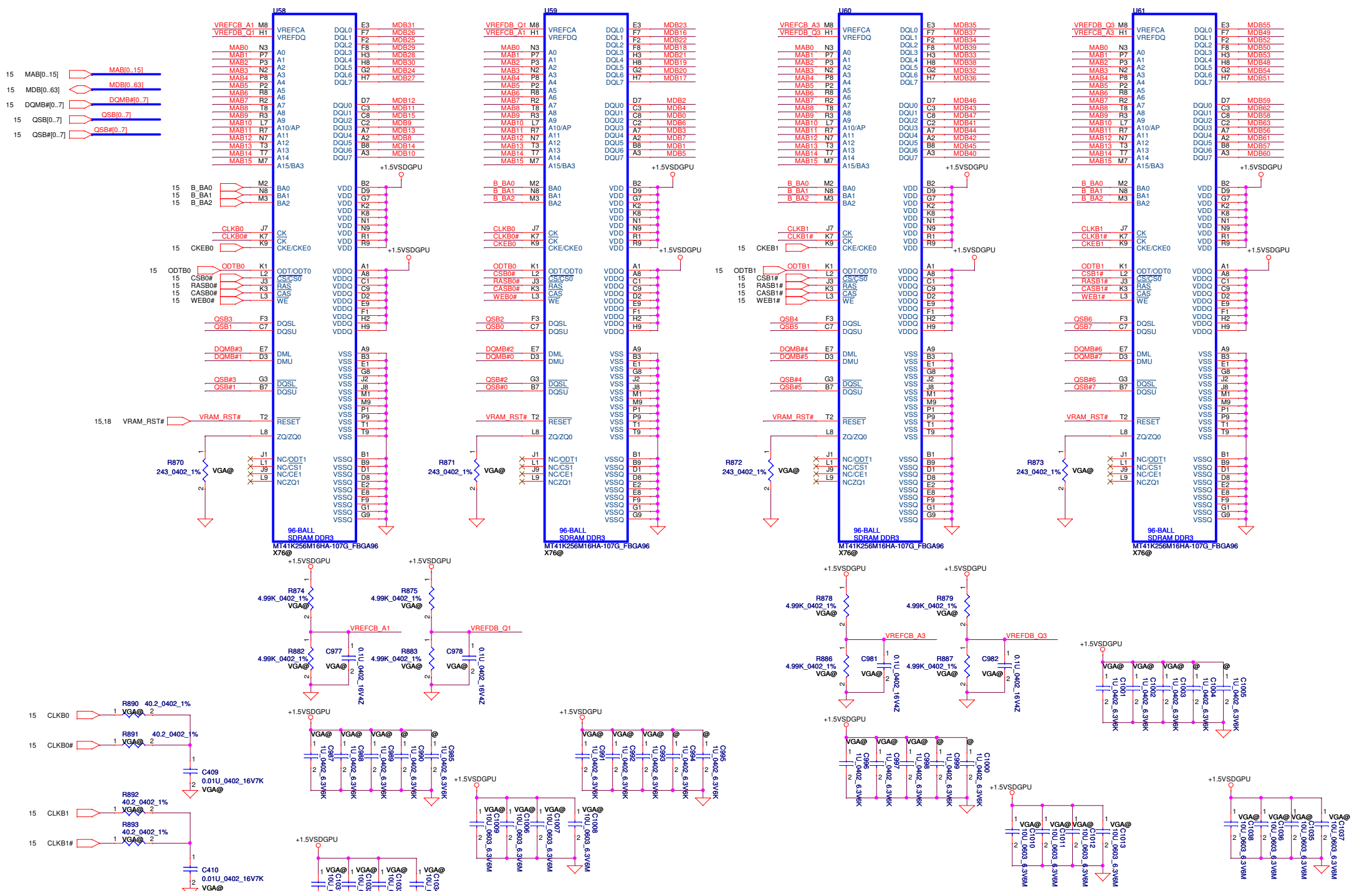
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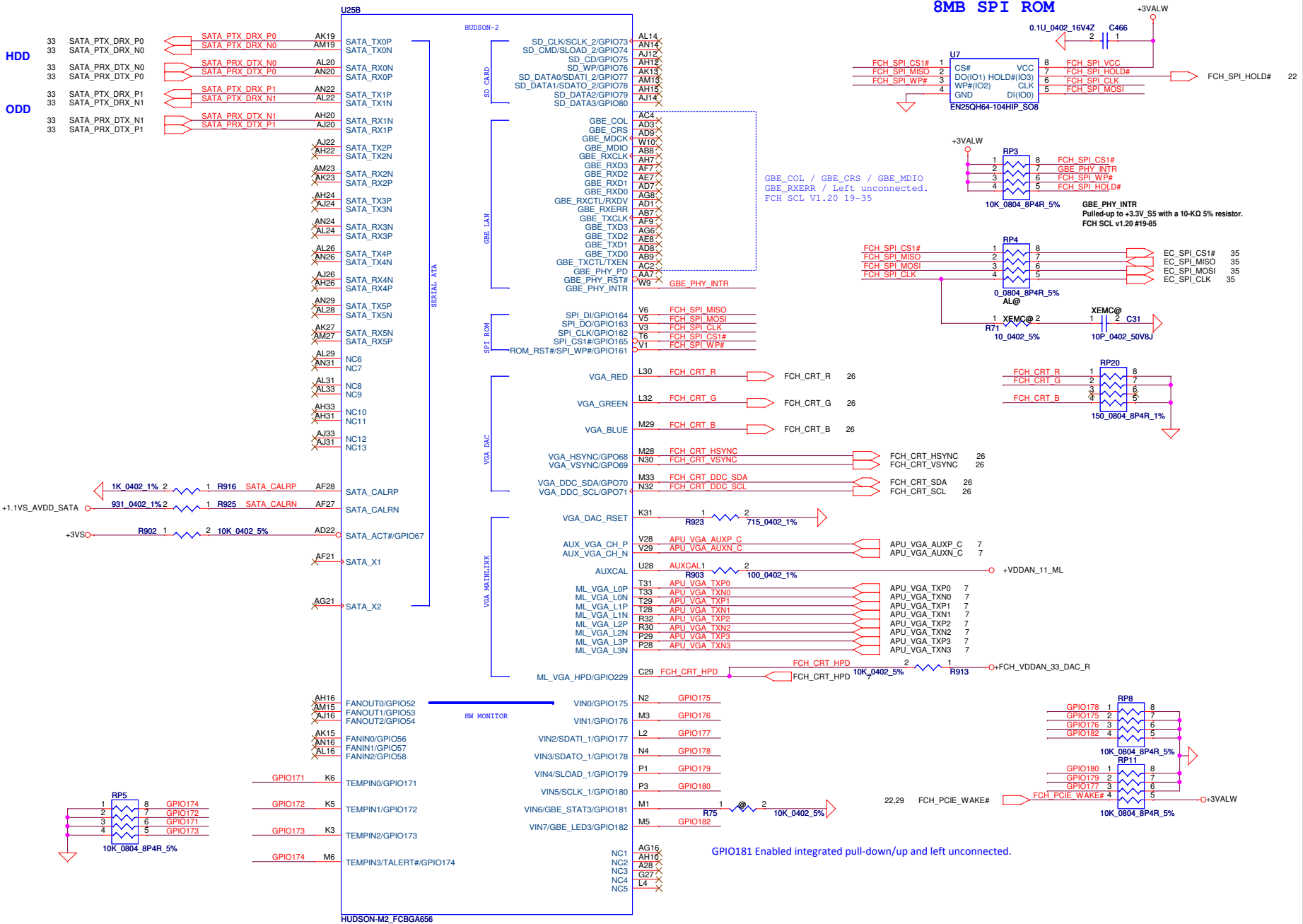


X76
ZZZ1
X76
X76550BOL41
HYN1G@
ZZZ2
X76
X76550BOL42
MRN1G@
ZZZ3
X76
X76550BOL43
SAM1G@
ZZZ4
X76
X76550BOL44
HYN2G@
ZZZ5
X76
X76550BOL45
MRN2G@
ZZZ6
X76
X76550BOL46
SAM2G@





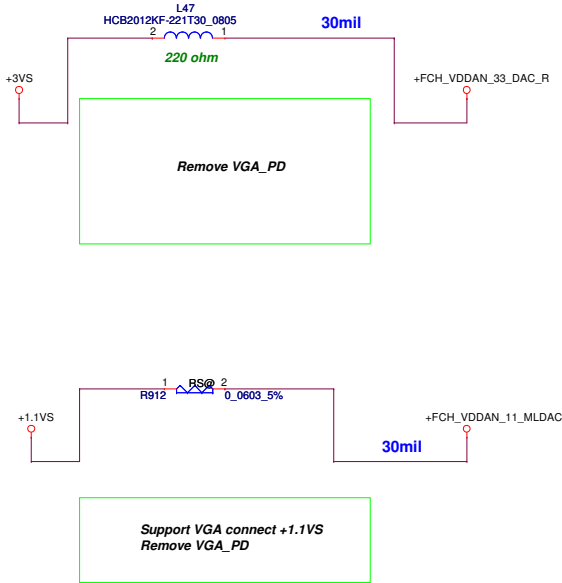
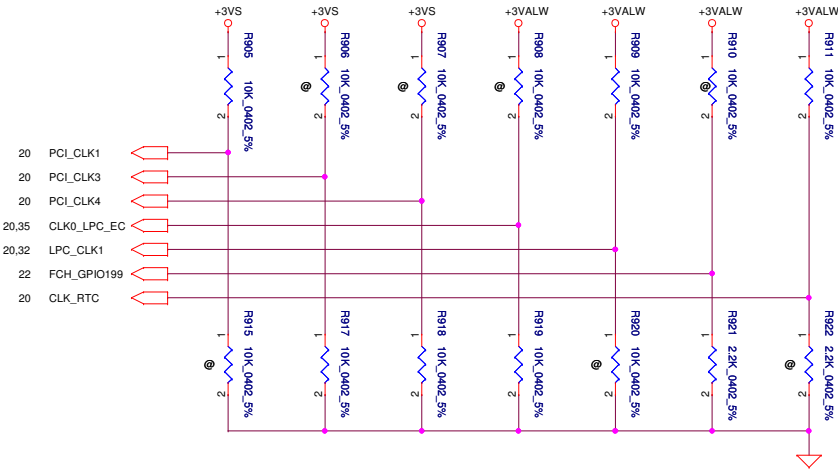
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				Bolton-M3-SATA/GBE/HWM
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STRAP PINS

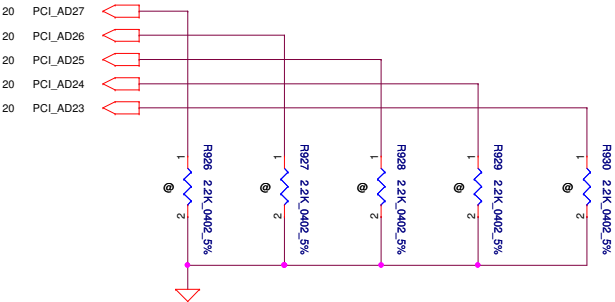
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	FCH_GPIO199	CLK_RTC
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	FCH EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	FCH EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



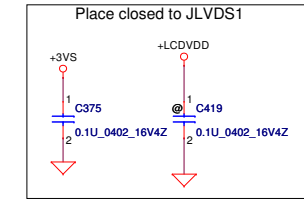
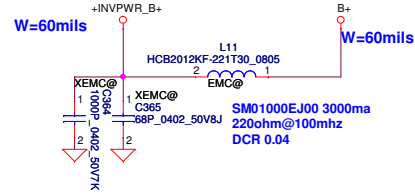
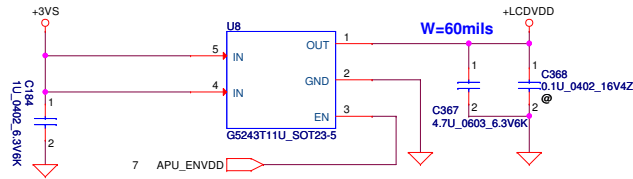
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

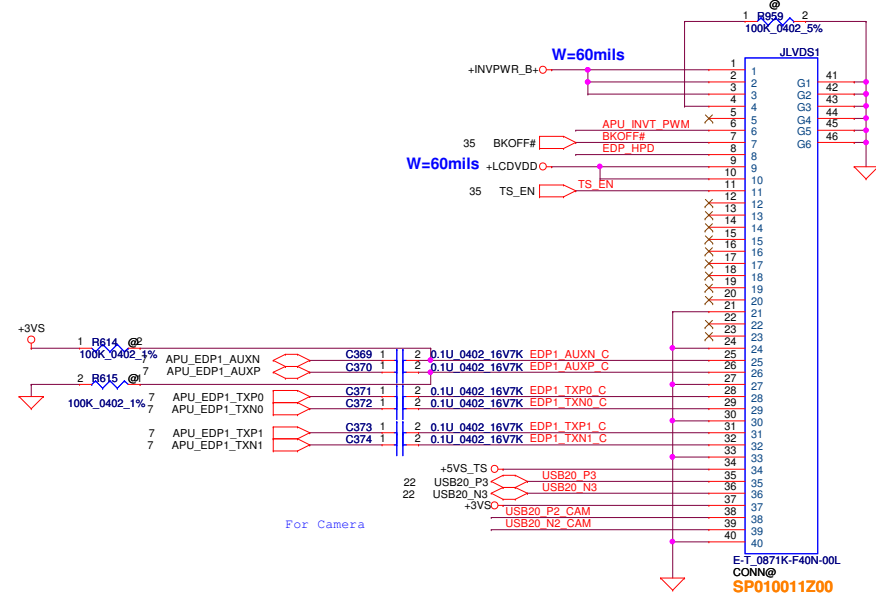
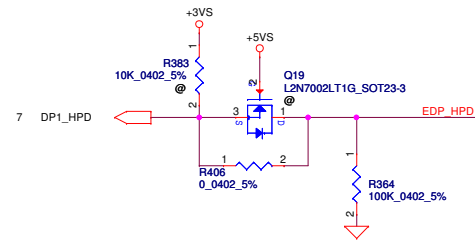
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	RESERVED DEFAULT	NORMAL REFCLK TERMINATION DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	RESERVED	INVERT REFCLK TERMINATION	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



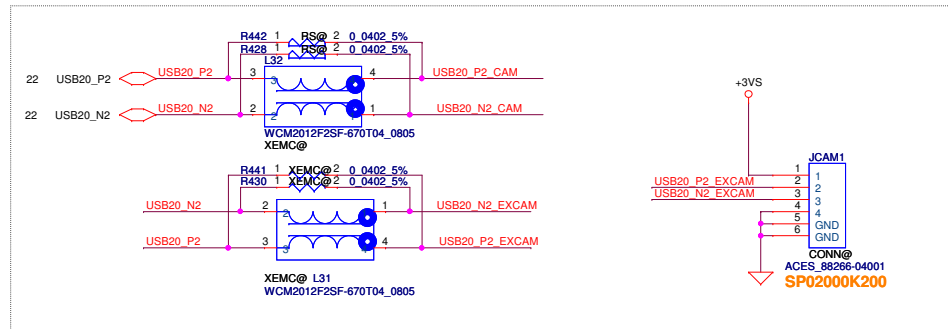
LCD POWER CIRCUIT



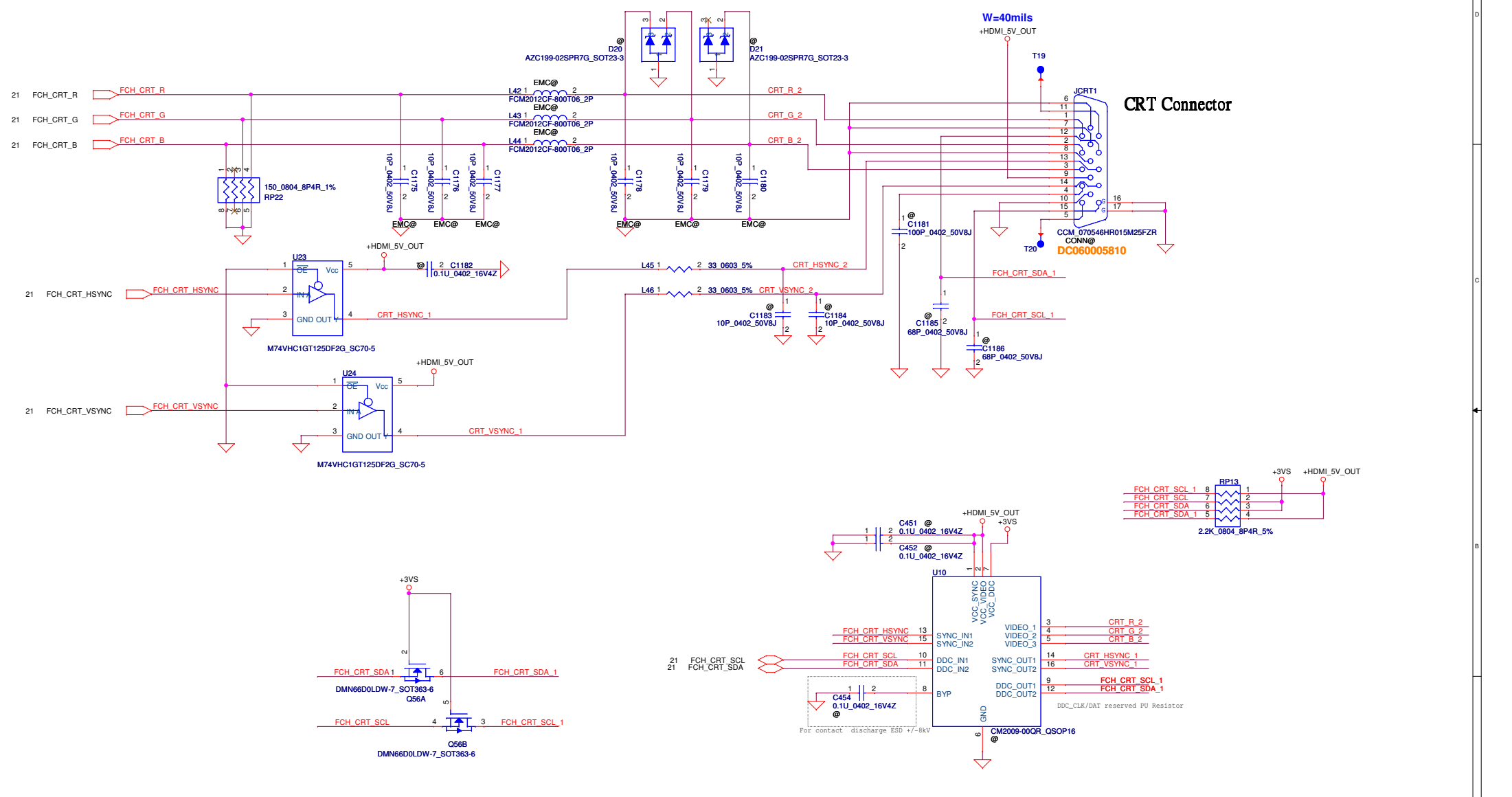
LCD/ LED PANEL Conn.



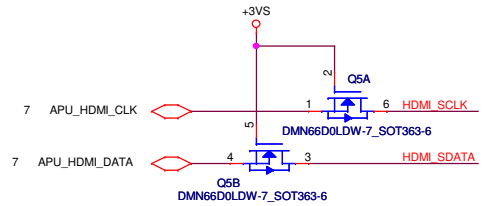
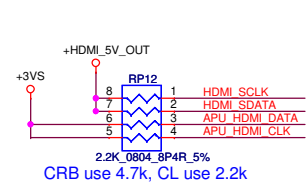
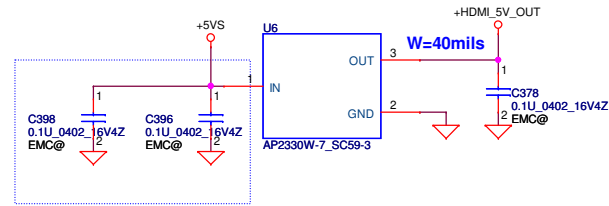
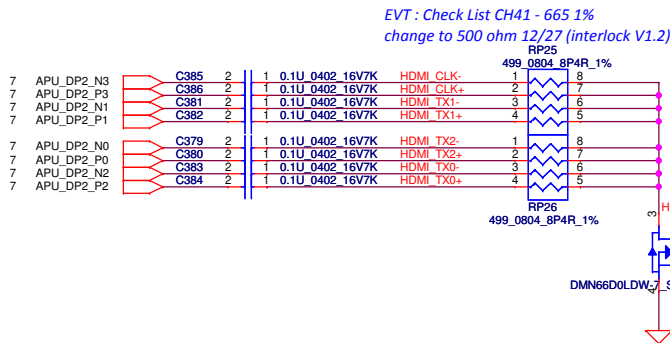
CMOS co-layout 4pin conn & eDP conn



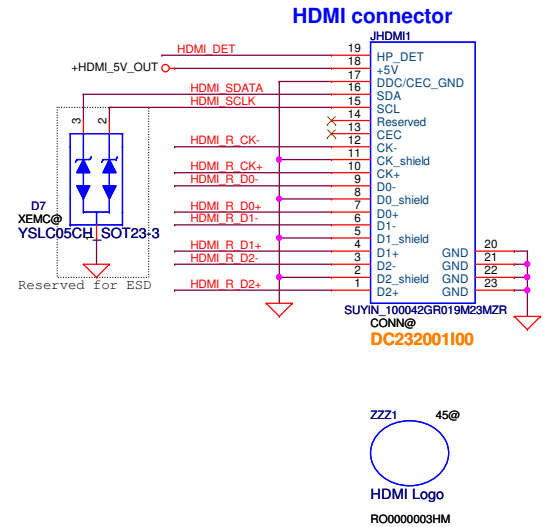
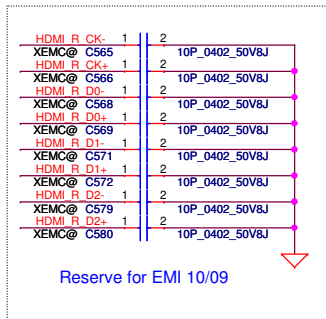
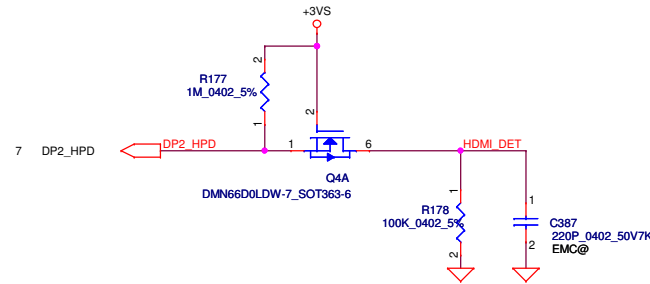
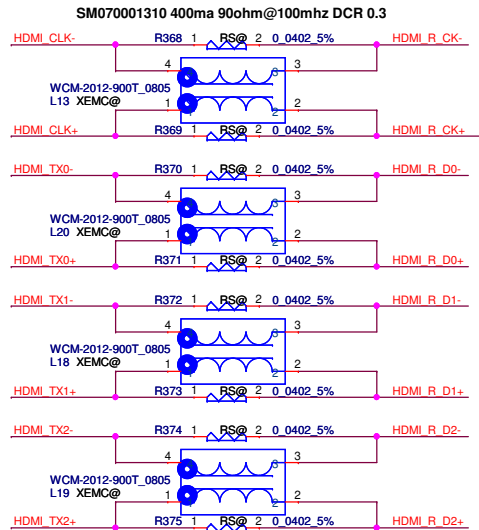
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Issued Date	2012/09/12	Deciphered Date	2012/07/29	Title	
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				Date:	Wednesday, February 12, 2014
				Sheet	26 of 52

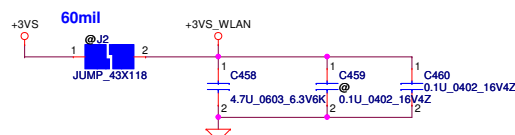
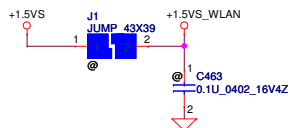
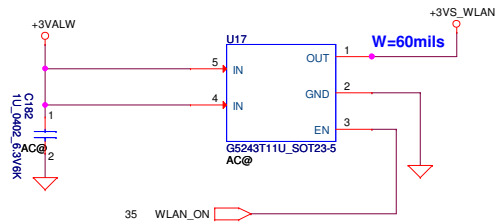


Reserved for ESD

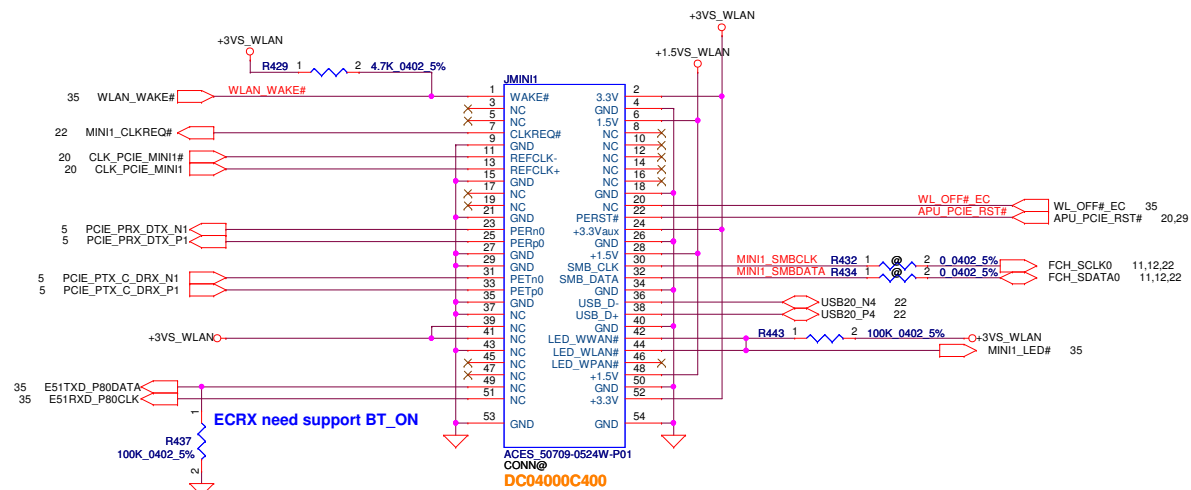


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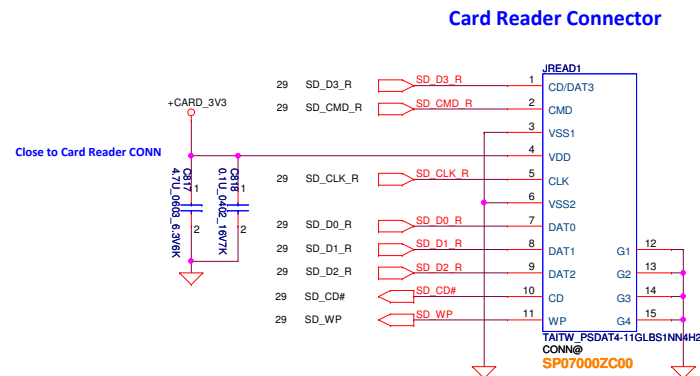
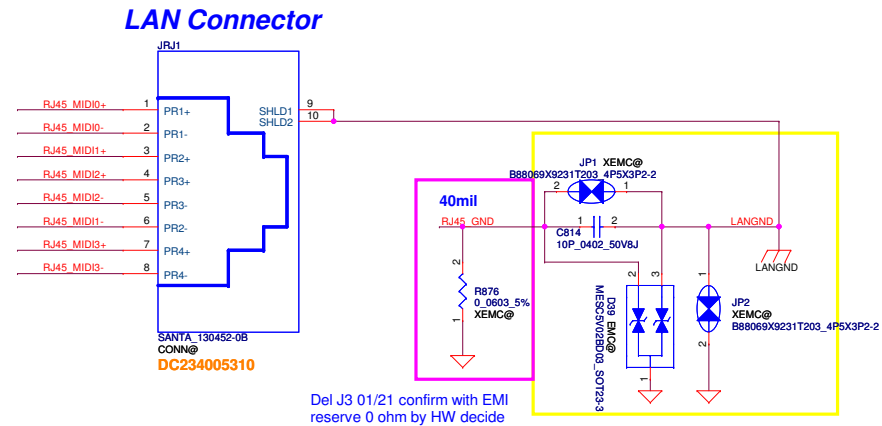
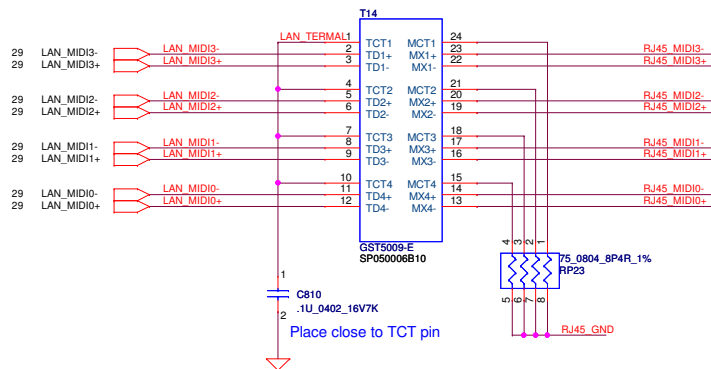
Mini-Express Card for WLAN/WiMAX(Half)



Mini-Express Card(WLAN) Mini Card Power Rating

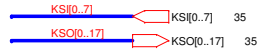


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Issued Date		2012/09/12		Deciphered Date		2012/07/29		MINI Card									
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								Document Number									
								Date:		Wednesday, February 12, 2014		Sheet		26		of 52	

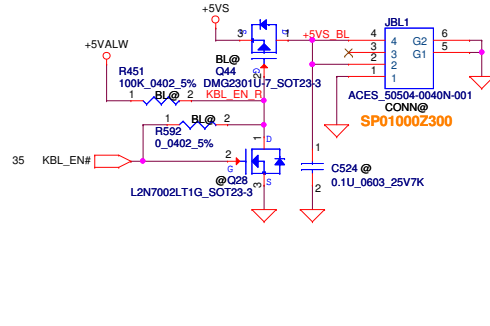


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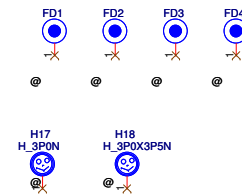
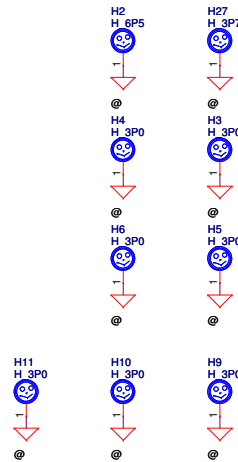
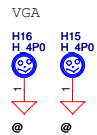
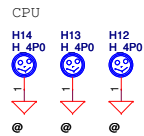
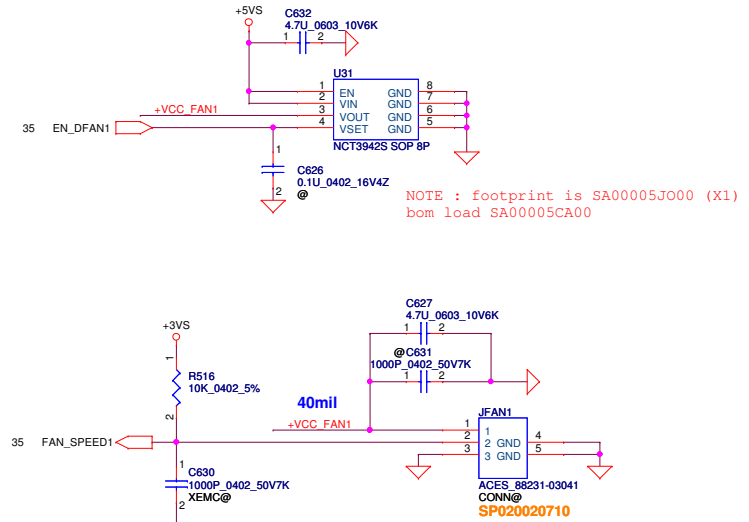
KB Conn.



KB BackLight Conn. Reserve

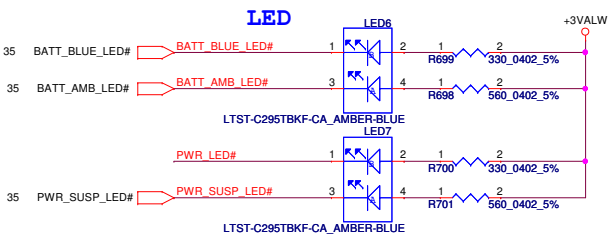


FAN1 Conn



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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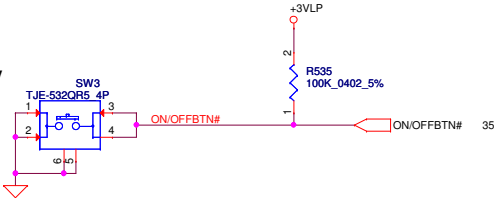
LED



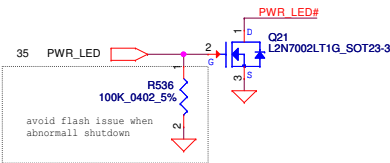
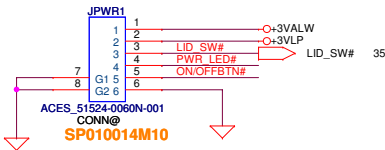
ON/OFF BTN

Test Only

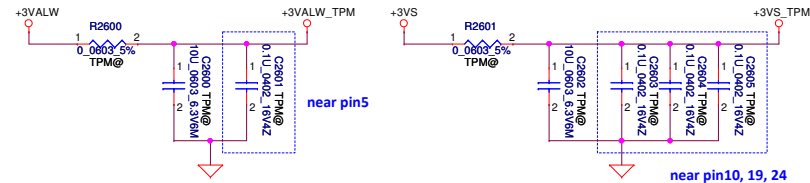
TOP



PWR/B



TPM Board



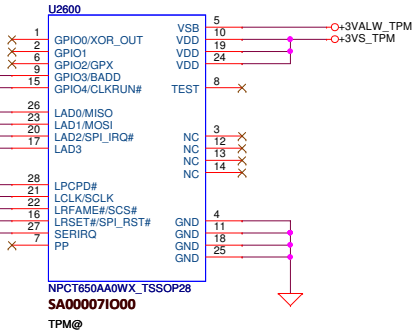
BADD	SELECTION
0	EEh - EFh
* 1	7Eh - 7Fh

GPIO3/BADD with Internal PH (default)

AMD CLKRUN# no need PH (DG1.1)

LPCPD# had internal PH

SERIRQ no need PH

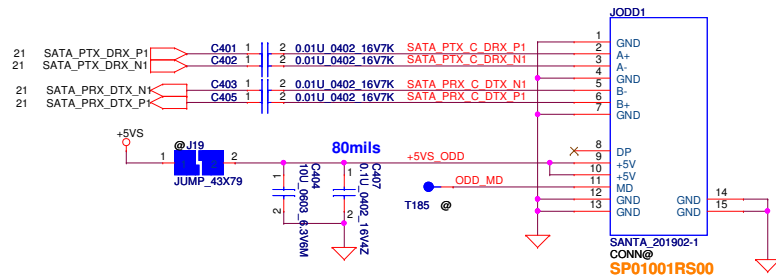


CLKRUN# PH request by TPM chip DG 1/22

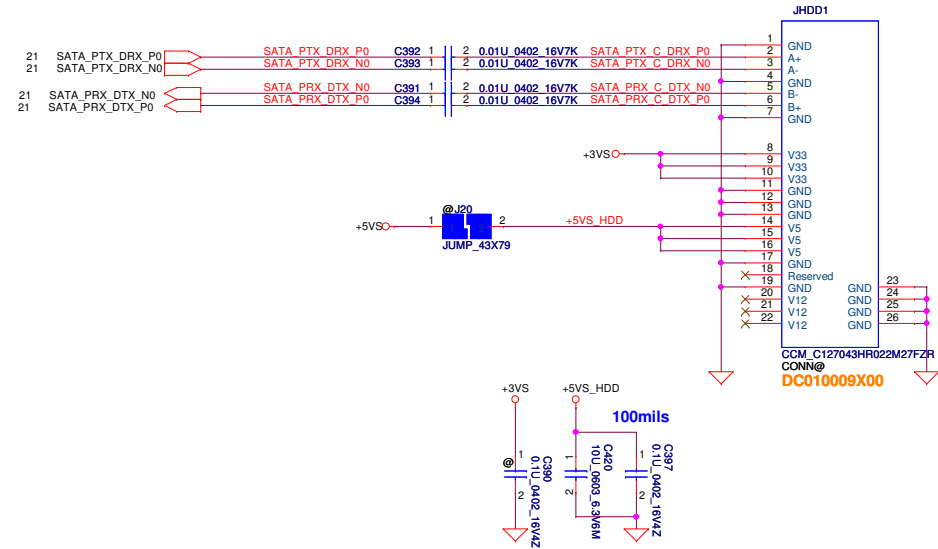
G-sensor

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				Z5WAK M/B LA-B221P	0.2
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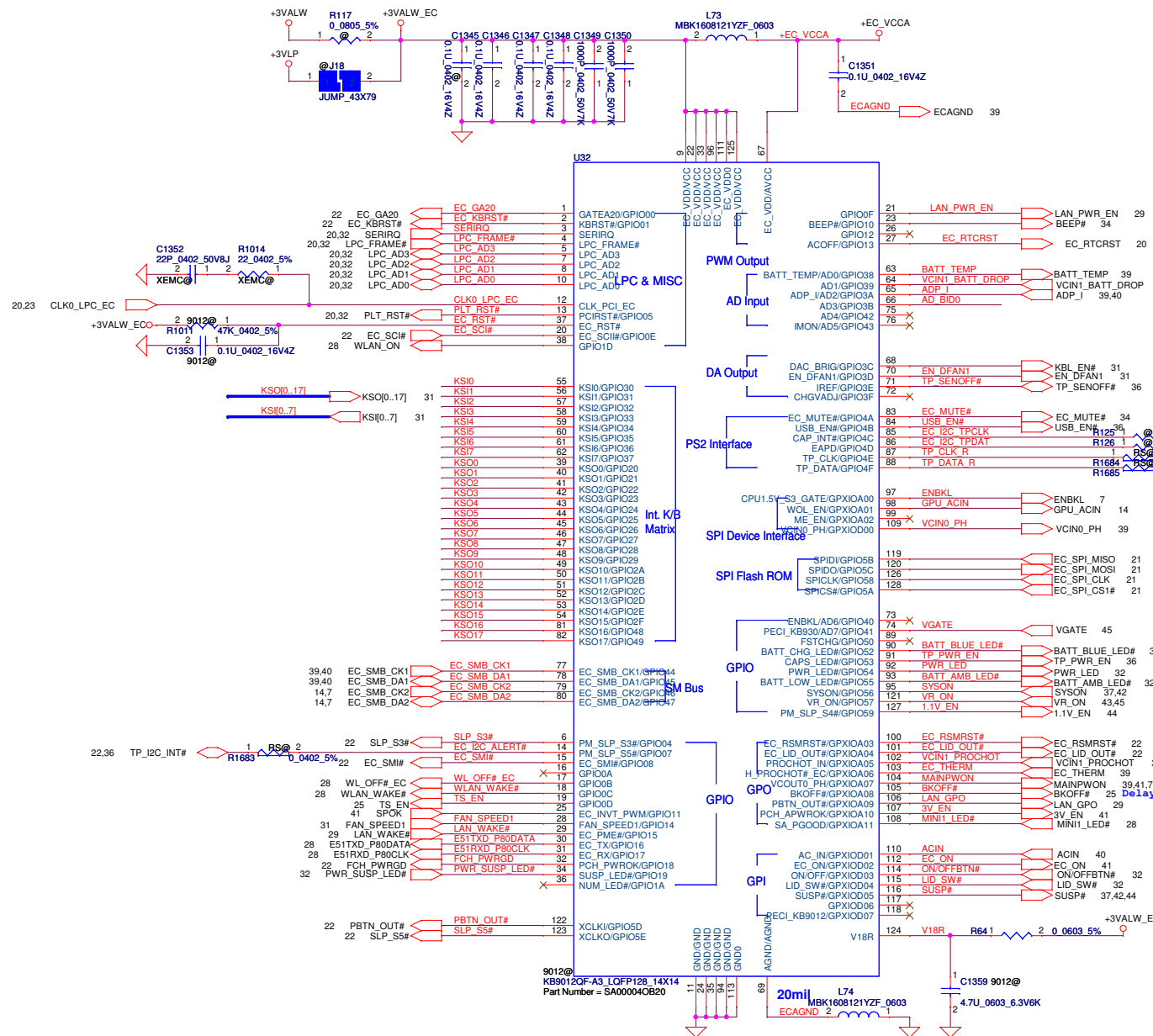
SATA ODD Conn.



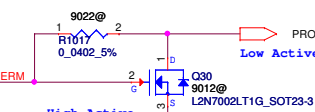
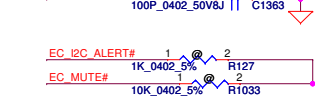
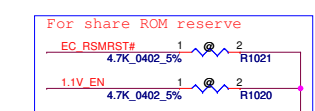
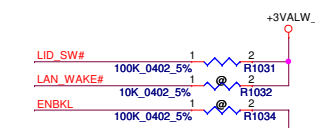
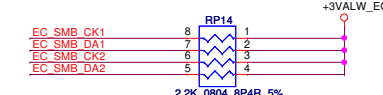
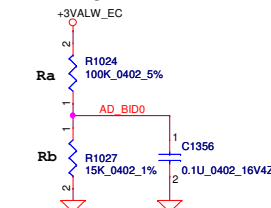
SATA HDD Conn.



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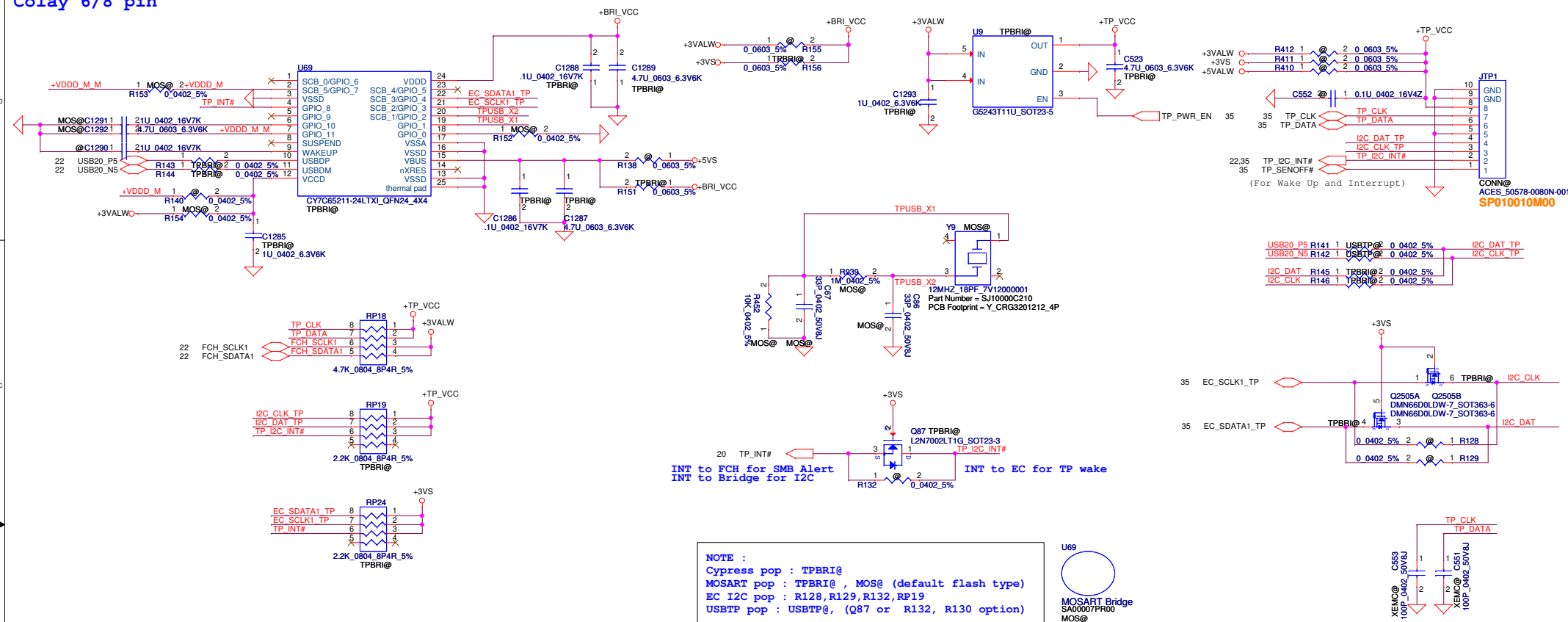
Analog Board ID definition



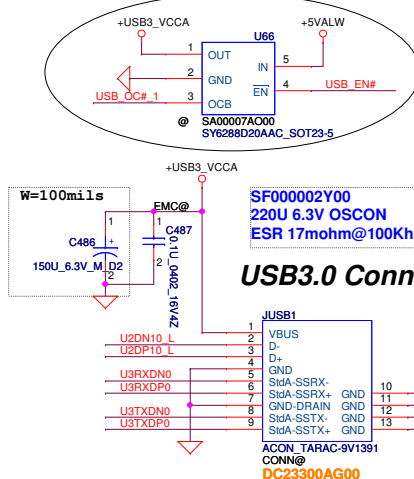
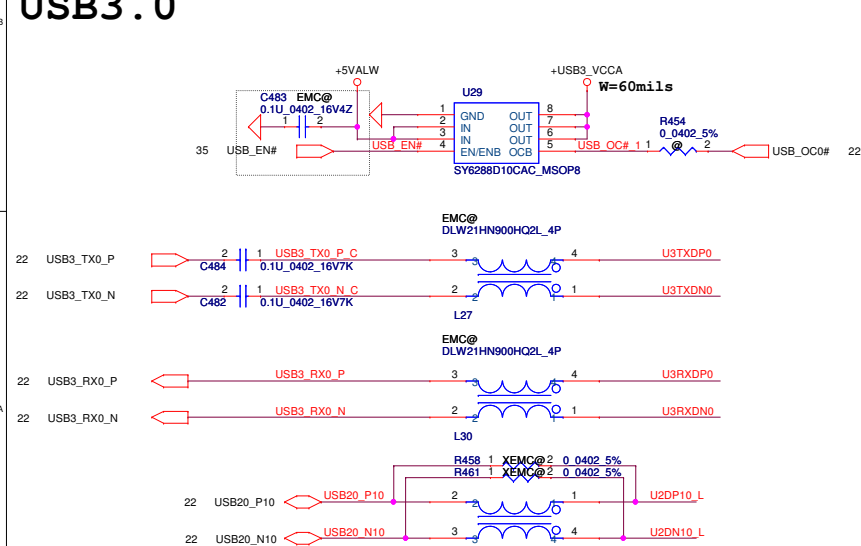
U32 9022@
SAA00075S20
KB9022CC-A3_LQFP128_14X14

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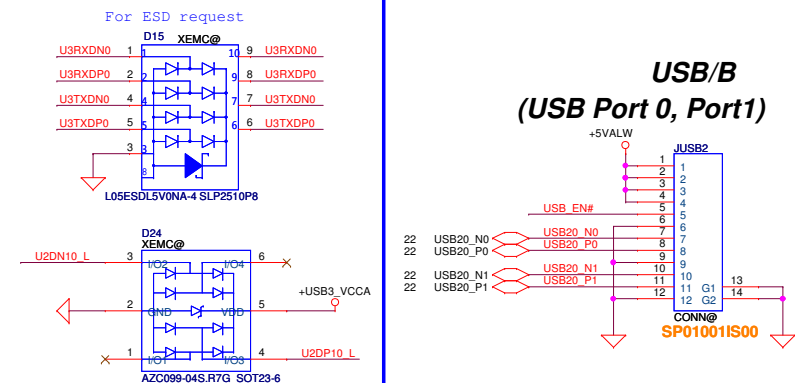
To TP/B Conn.
Colay 6/8 pin



USB3.0

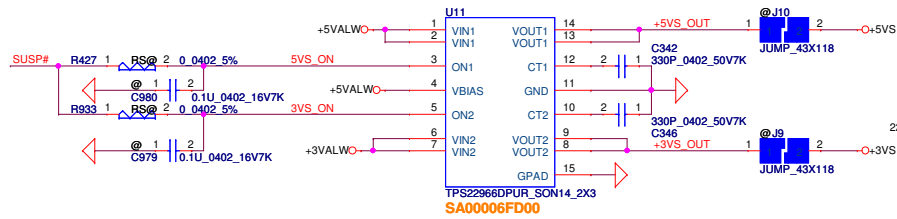


USB2.0 CONN

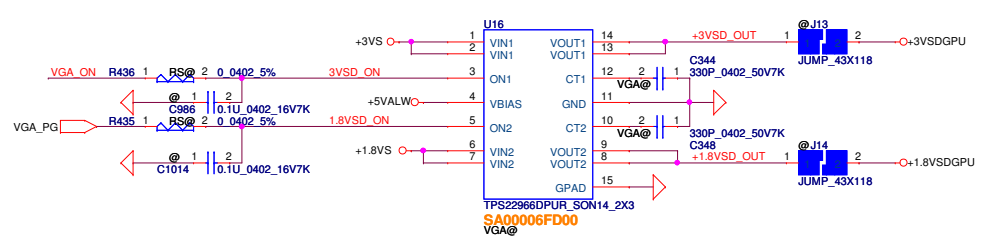


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				Document Number Z5WAK M/B LA-B221P	
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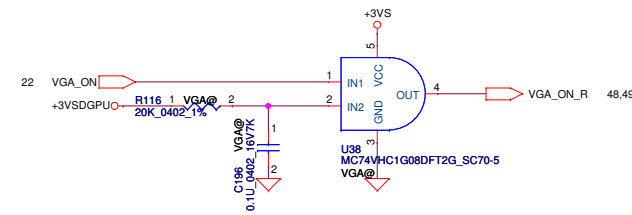
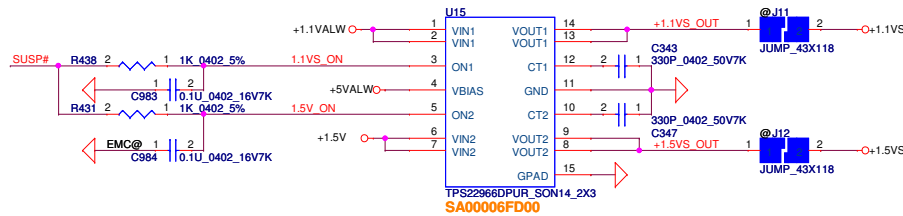
+5VALW to +5VS
+3VALW to +3VS



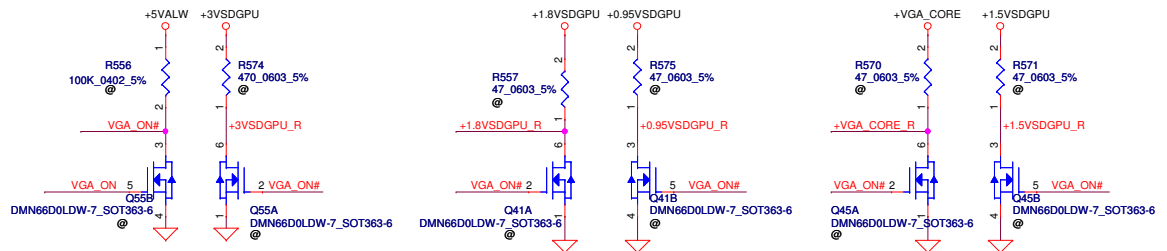
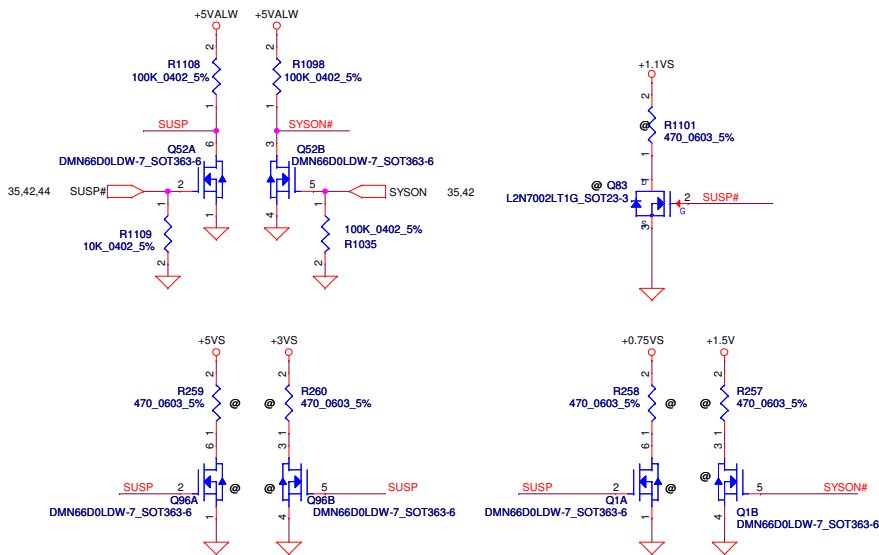
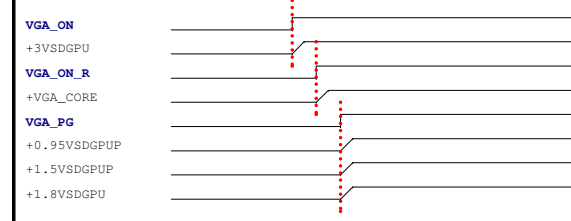
+3VS to +3VSDGPU
+1.8VS to +1.8VSDGPU



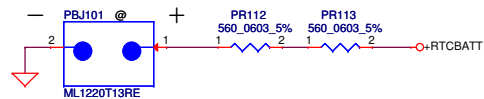
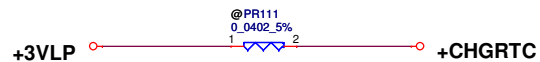
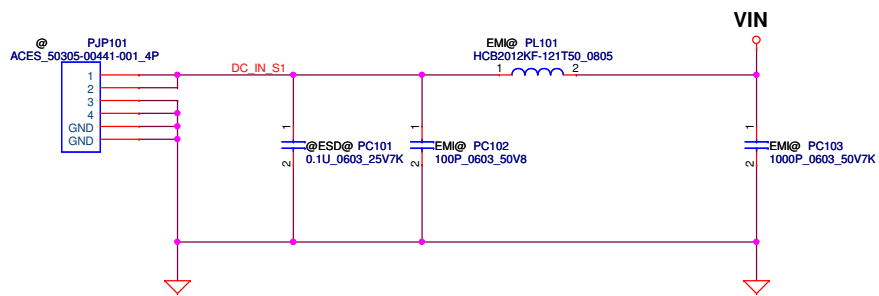
+1.1VALW to +1.1VS
+1.5V to +1.5VS



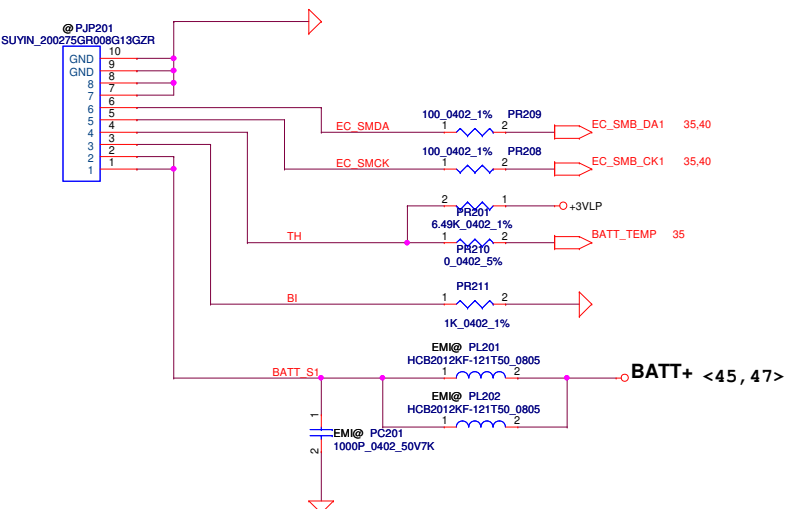
VGA sequence : default same as V5WE2
(0.95V can be option before VGA_CORE)



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				Document Number	Rev
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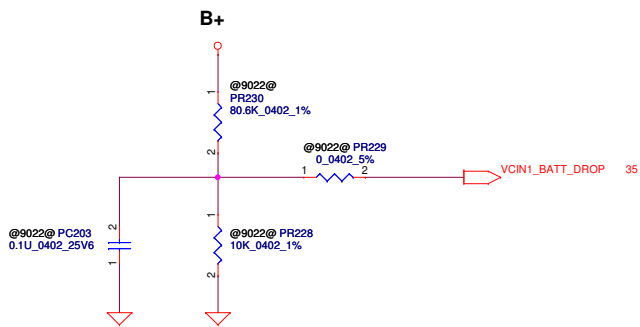
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				Custom		0.3
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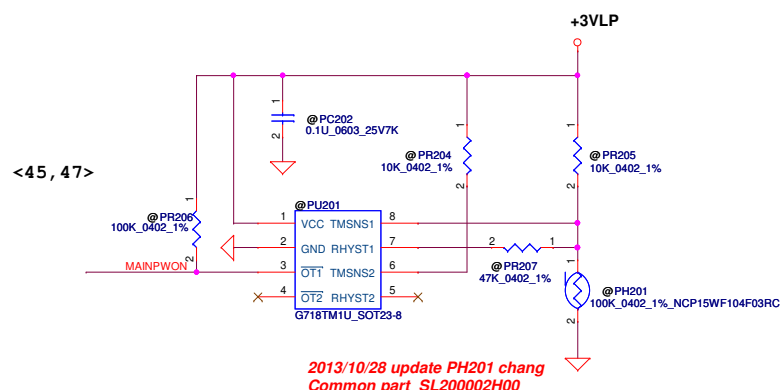
---Battery_pin define---
 PIN1 GND
 PIN2 GND
 PIN3 SMD
 PIN4 SMC
 PIN5 TS
 PIN6 B/I
 PIN7 Batt+
 PIN8 Batt+
 ---Battery Con_pin define---
 PIN8 GND
 PIN7 GND
 PIN6 SMD
 PIN5 SMC
 PIN4 TS
 PIN3 B/I
 PIN2 Batt+
 PIN1 Batt+

2013/10/02
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

Battery is 3-cell design.
B+=9V



For 40W adapter==>action 42.8W , Recovery 34.4W
 42.8W:
 $I_{ada} = 0 \sim 2.253A$ ($42.8W/19V = 2.253A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 2.253 * 0.02 = 0.901$
 34.4W:
 $I_{ada} = 0 \sim 1.811A$ ($34.4W/19V = 1.811A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 1.811 * 0.02 = 0.724$
 $CP = 40W * 0.85 = 34W$
 For 65W adapter==>action 69.55W , Recovery 55.9W
 69.55W:
 $I_{ada} = 0 \sim 3.661A$ ($69.55W/19V = 3.661A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 3.661 * 0.02 = 1.464$
 55.9W:
 $I_{ada} = 0 \sim 2.942A$ ($55.9W/19V = 2.942A$)
 $ADP_I = 20 * I_{ada} * R_{sense}$
 $ADP_I = 20 * 2.942 * 0.02 = 1.177$
 $CP = 65W * 0.85 = 55.25W$

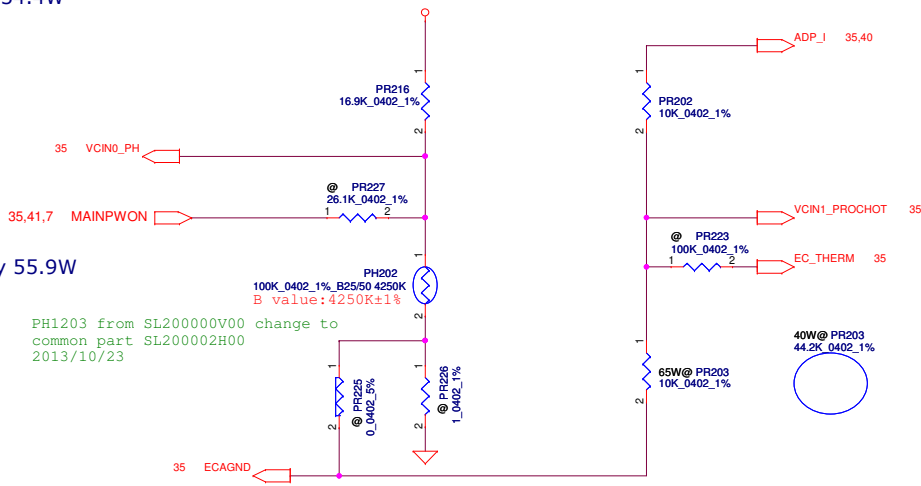


2013/10/28 update PH201 chang
Common part SL200002H00

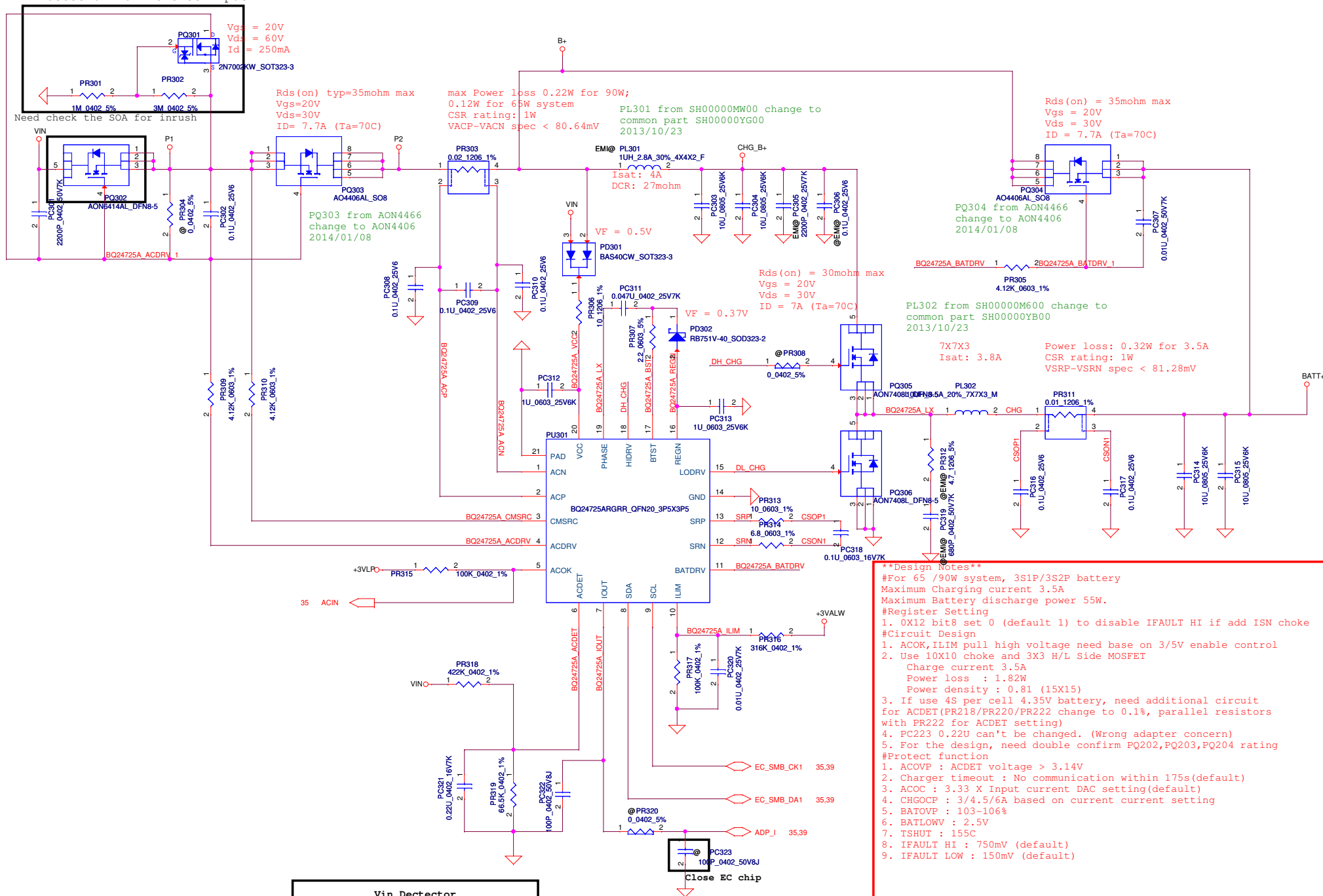
For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	92C, 1V	56C, 2.044V
PH202 (ohm)	6.99K	26.03K

For KB9012 sense 20mΩ	Active	Recovery
40W	42.8W, 0.73V	34.4W, 0.59V
65W	69.55W, 0.73V	55.9W, 0.59V

PH201 under CPU botten side :
 CPU thermal protection at 92 degree C (shutdown)
 Recovery at 56 degree C +EC_VCCA



Protection for reverse input



Vin Dectector			
	Min.	Typ	Max.
L--->H	17.16V	17.63V	18.12V
H--->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
 ILIM = $3.3 \times 100 / (100 + 107) / 20 / 0.02$
 = 986 A

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				Date:	Wednesday, February 12, 2014	Sheet 40 of 53

Module model information

SY8208B_V2.mdd
SY8208C_V2.mdd

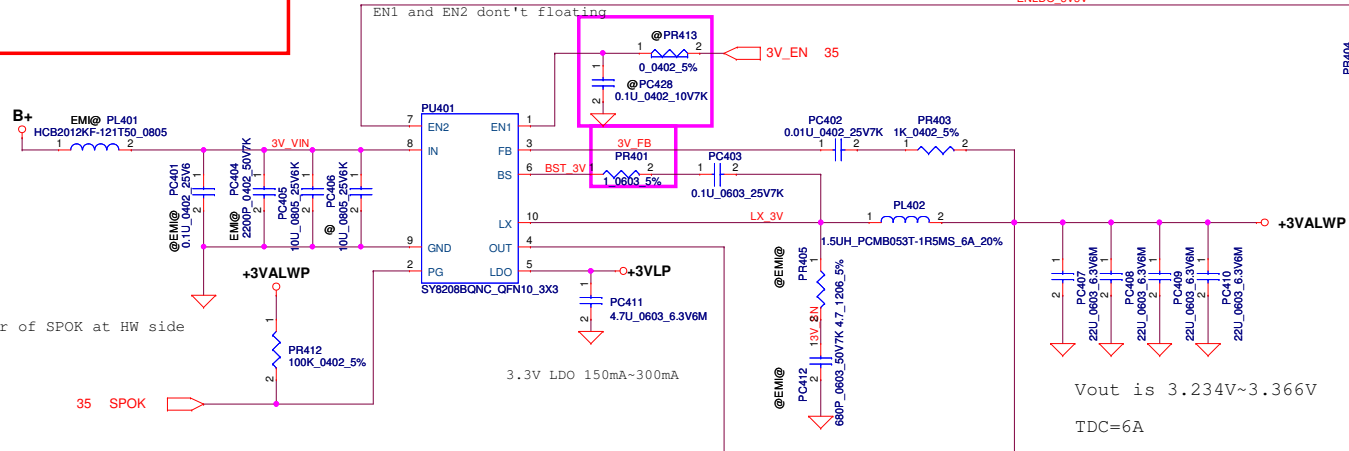
PR401 FAE review : change from
2.2_0603_5% to 1_0603_5%
HW request add PR413,
and PC428-un-pop

EN1 and EN2 don't floating

EN1 and EN2 don't floating

ENLDO 3V5V

PR402
499K 0402 1%
B+

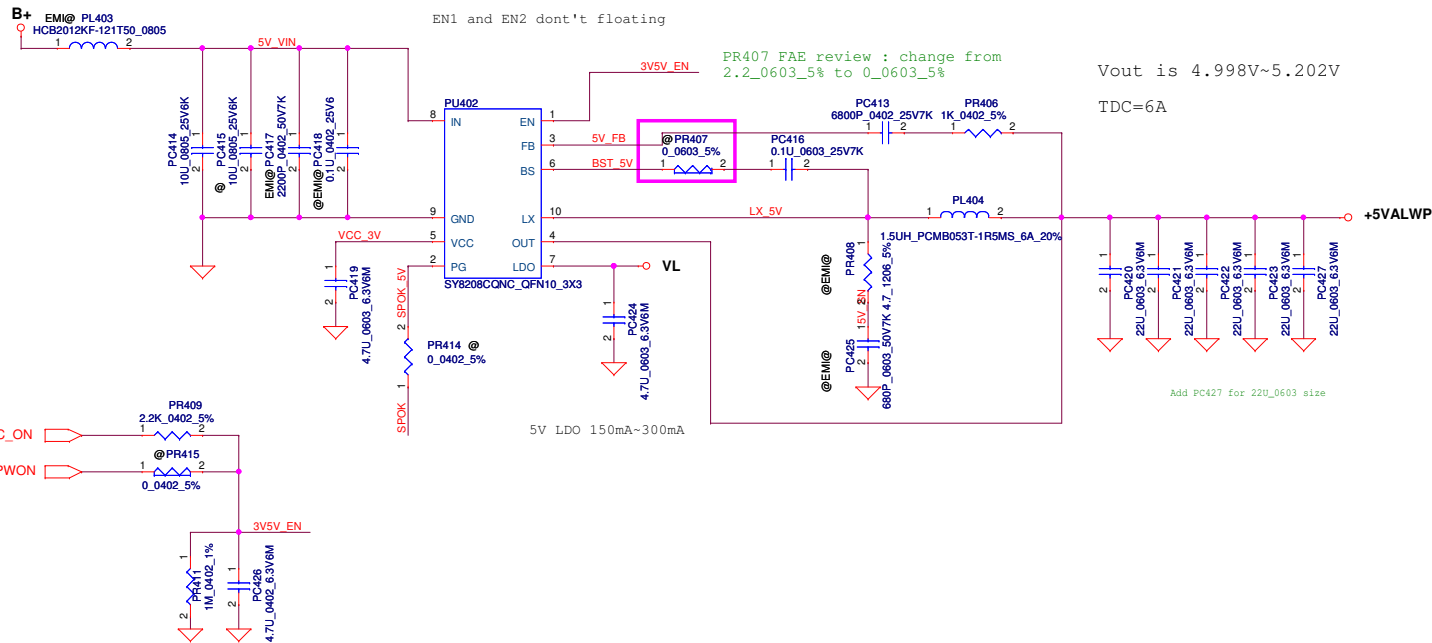


Vout is 3.234V~3.366V

TDC=6A

+3VALWP @PJ401
JUMP_43X118 +3VALW

+5VALWP @PJ402
JUMP_43X118 +5VALW



Vout is 4.998V~5.202V

TDC=6A

Add PC427 for 22U_0603 size

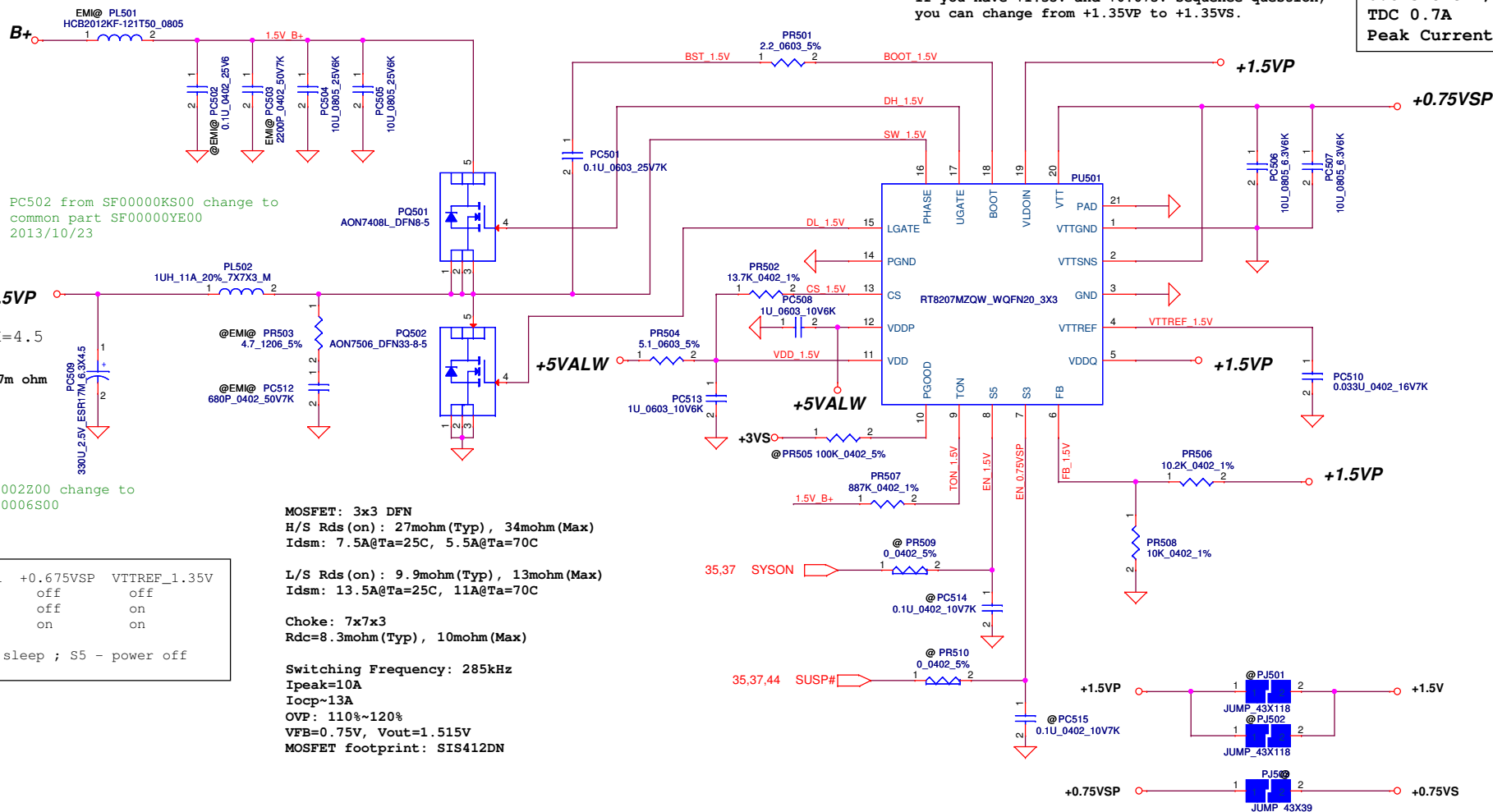
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Issued Date				2011/06/15				Title			
Deciphered Date				2013/10/01				+3VALW/+5VALW			
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Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

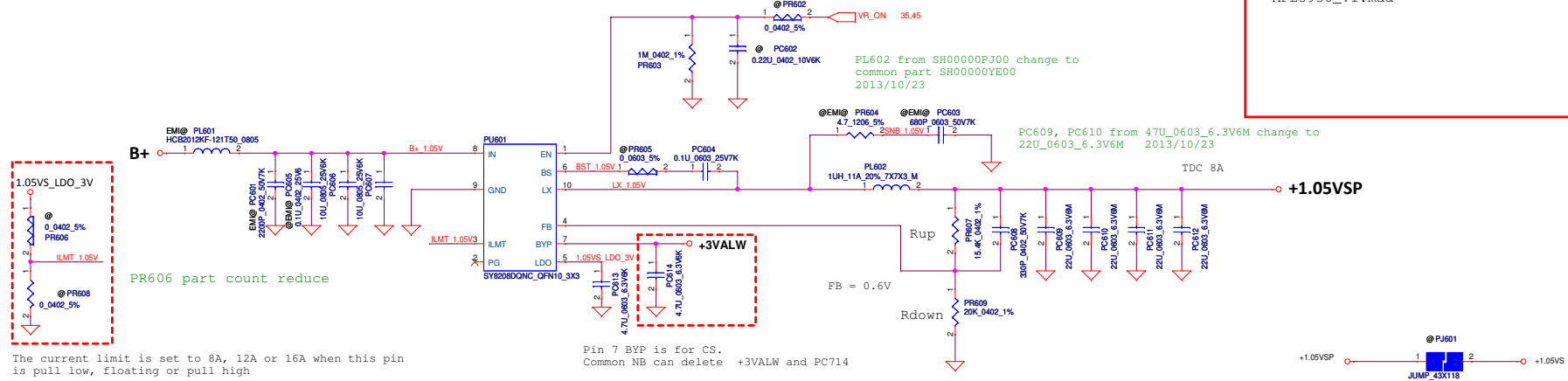
0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2010/07/20		Deciphered Date		2013/10/01		Title			
								+1.5VP/+0.75VSP			
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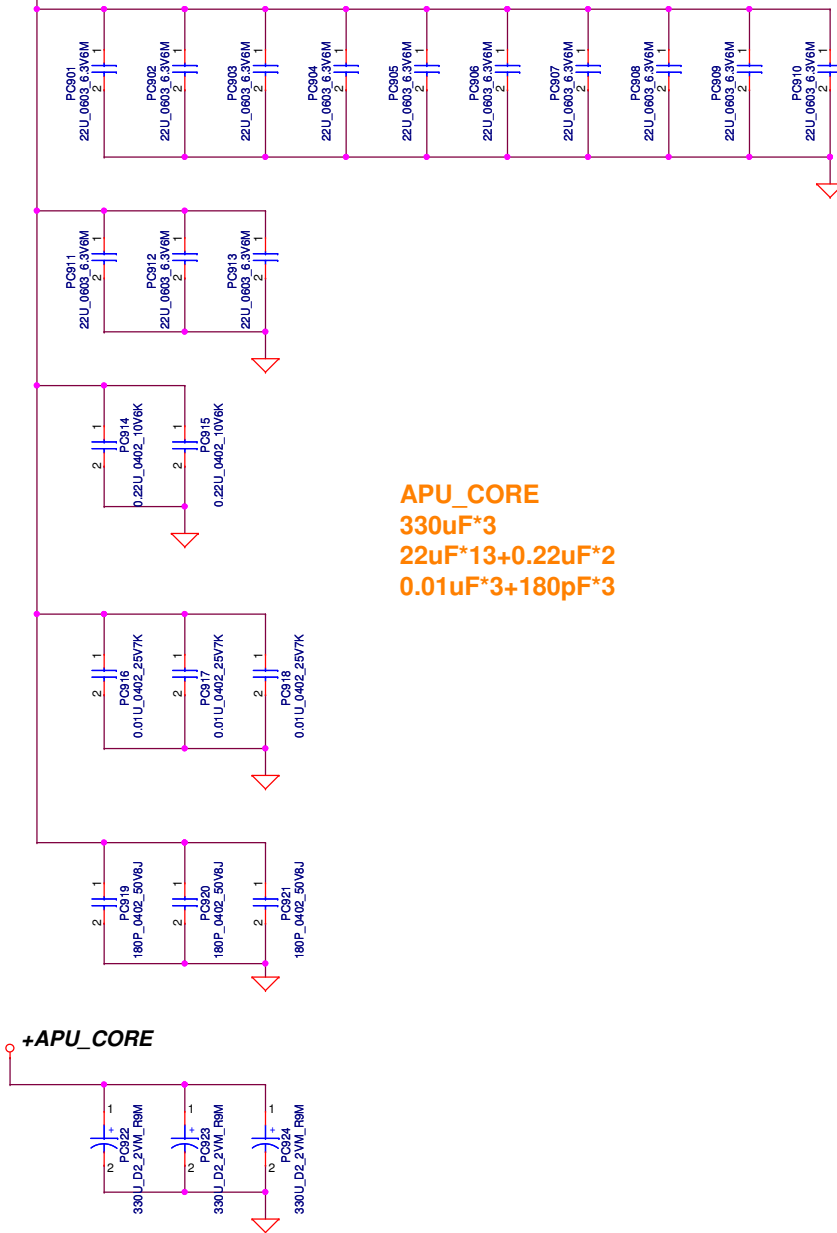
EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

Module model information
SY8208D_V1.mdd
APL5930_V1.mdd



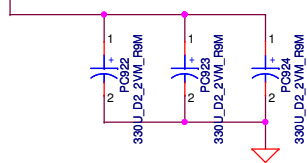
+APU_CORE

+APU_CORE



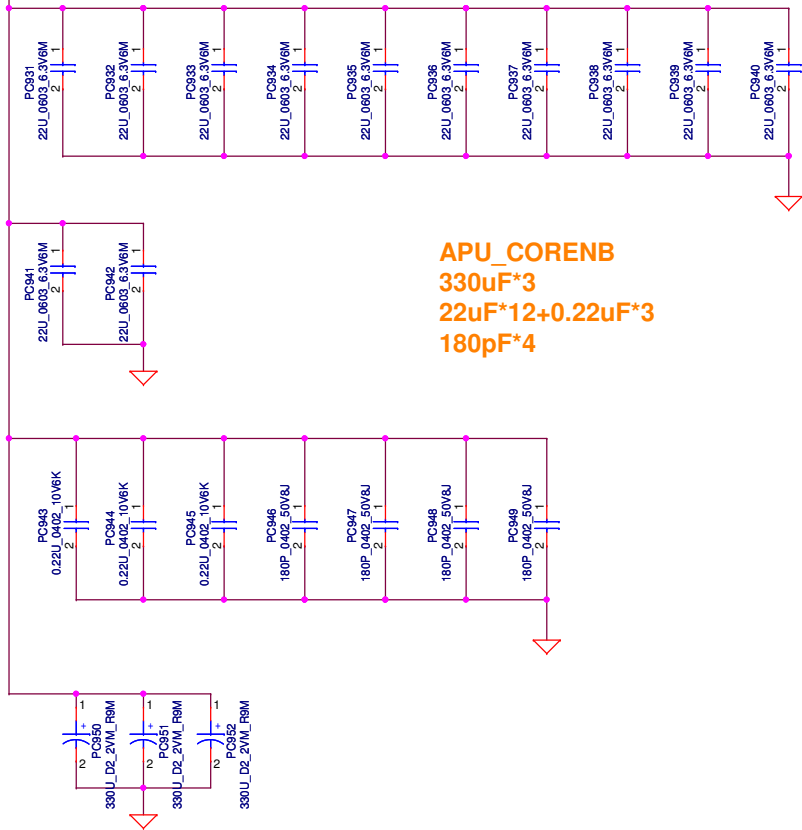
APU_CORE
330uF*3
22uF*13+0.22uF*2
0.01uF*3+180pF*3

+APU_CORE



+APU_CORE_NB

+APU_CORE_NB



APU_CORENB
330uF*3
22uF*12+0.22uF*3
180pF*4

Security Classification		Compal Secret Data		Title	
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				VS50 AMD	
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Module model information

TPS51212_V1.mdd for Single layer
TPS51212_V2.mdd for Dual layer

Resistance(KΩ)	Frequency(KHz)
470	290
200	340
100	380
39	430

MOSFET: 3x3 DFN
H/S Rds (on): 24mohm(Typ), 30mohm(Max)
Id: 8.7A@Ta=25C, 7A@Ta=70C

L/S Rds (on): 13.5mohm(Typ), 16.5mohm(Max)
Idsm: 12A@Ta=25C, 9.5A@Ta=70C

Choke: 7x7x3
Rdc=15.5mohm +/-15%

+1.2V

Switching Frequency: 290kHz
Imax=8A
OCP~10.5A
OVP: 120%~130%
VFB=0.704V, Vout=1.207V

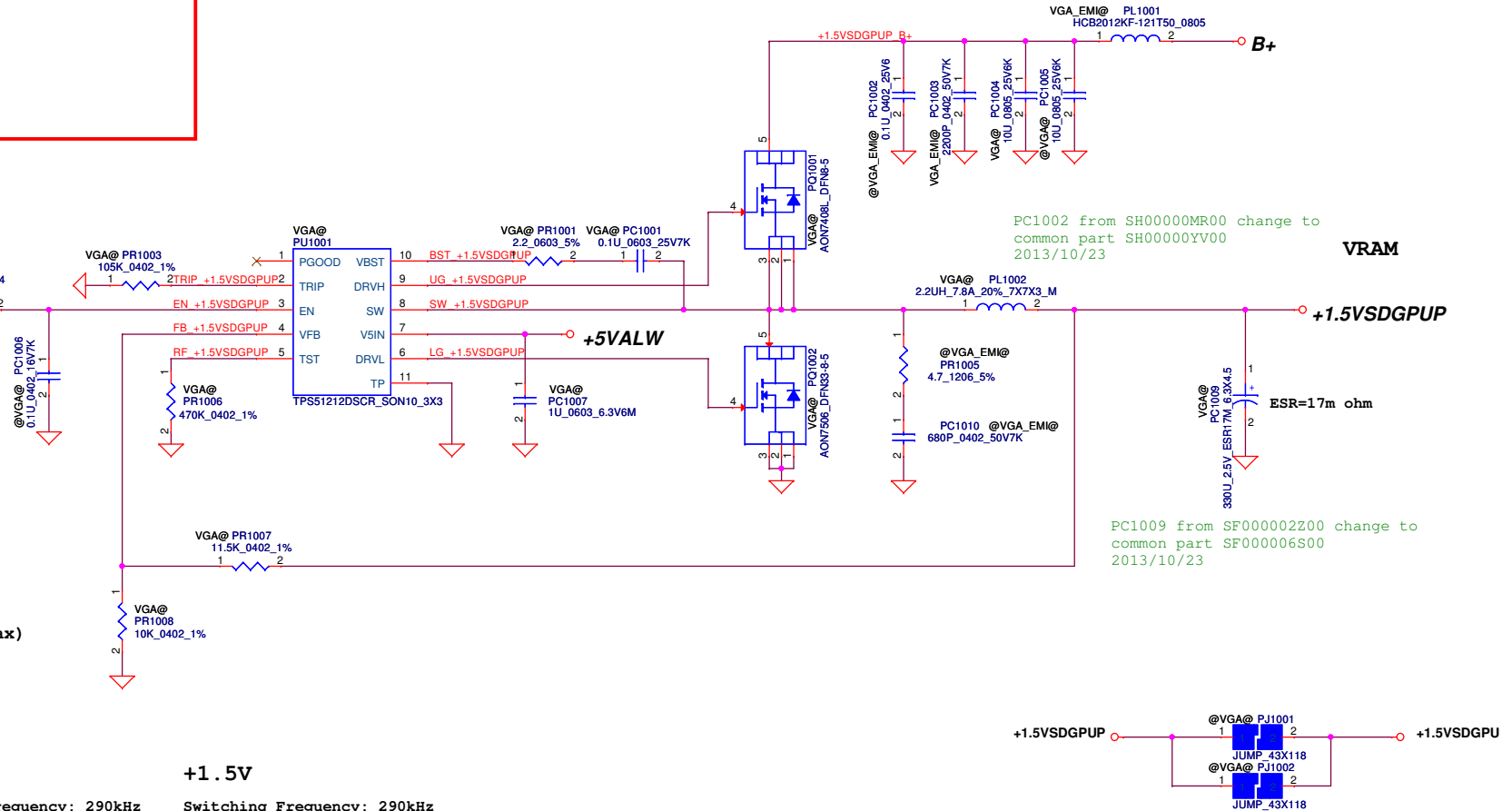
+1.05V

Switching Frequency: 290kHz
Imax=5.4A
Ipeak=6.5A
Iocp=7.8A
OVP: 120%~130%
VFB=0.704V, Vout=1.055V

+1.5V

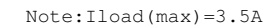
Switching Frequency: 290kHz
Imax=8A
OCP~10.5A
OVP: 120%~130%
VFB=0.704V, Vout=1.514V

Vout	PR1007	PR1008	PR1003
+1.2V	7.15K	10k	105K
+1.05V	4.99k	10k	93.1k
+1.5V	11.5K	10k	105K

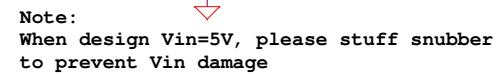


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SY8033_V1.mdd



HW request Add PR1107,
and unpop PR1104



$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

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				Custom		
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Vboc

- 1. PWM3 (Pin24) tie to 5V & CLK# (Pin40) external pull high
=> 2 phase CPU VR config
- PWM3 (Pin24) tie to 5V & CLK# (Pin40) tie to GND or floating
=> 2 phase GPU VR config

3. Bias=147K \rightarrow overshoot reduction function

37.48 VGA ON R

$$R_{th} = 12.02K$$
Recovery: $(6.98K + R_{th}) \cdot 56\mu A = 1.24V$

=> Tr=105C (+3C) 14 GPU_DPRSLPVR

protect T	protect T	
-----------	-----------	--

1999-2000	2000-2001

105C +3	96C +3
---------	--------

```
Rfset(kohm)=[period(us)-0.29]*2.65
```

 $f_{sw} = 1/\text{period}(\mu s) = 400\text{KHz}$

Common part SL200002E00

Figure 1. The study area.

PH1201 should place near
phase1 H-side MOS +3VSD

Rth

[illegible]

50 V 7

PO
p. 04
2

VGAPC1216

UCA@ PC1310 UCA@ PB1033

100

for positive shock

+VGA_CORE

16 VCC_GPU_SENSE

10. VCC_CPU_GENSE

100

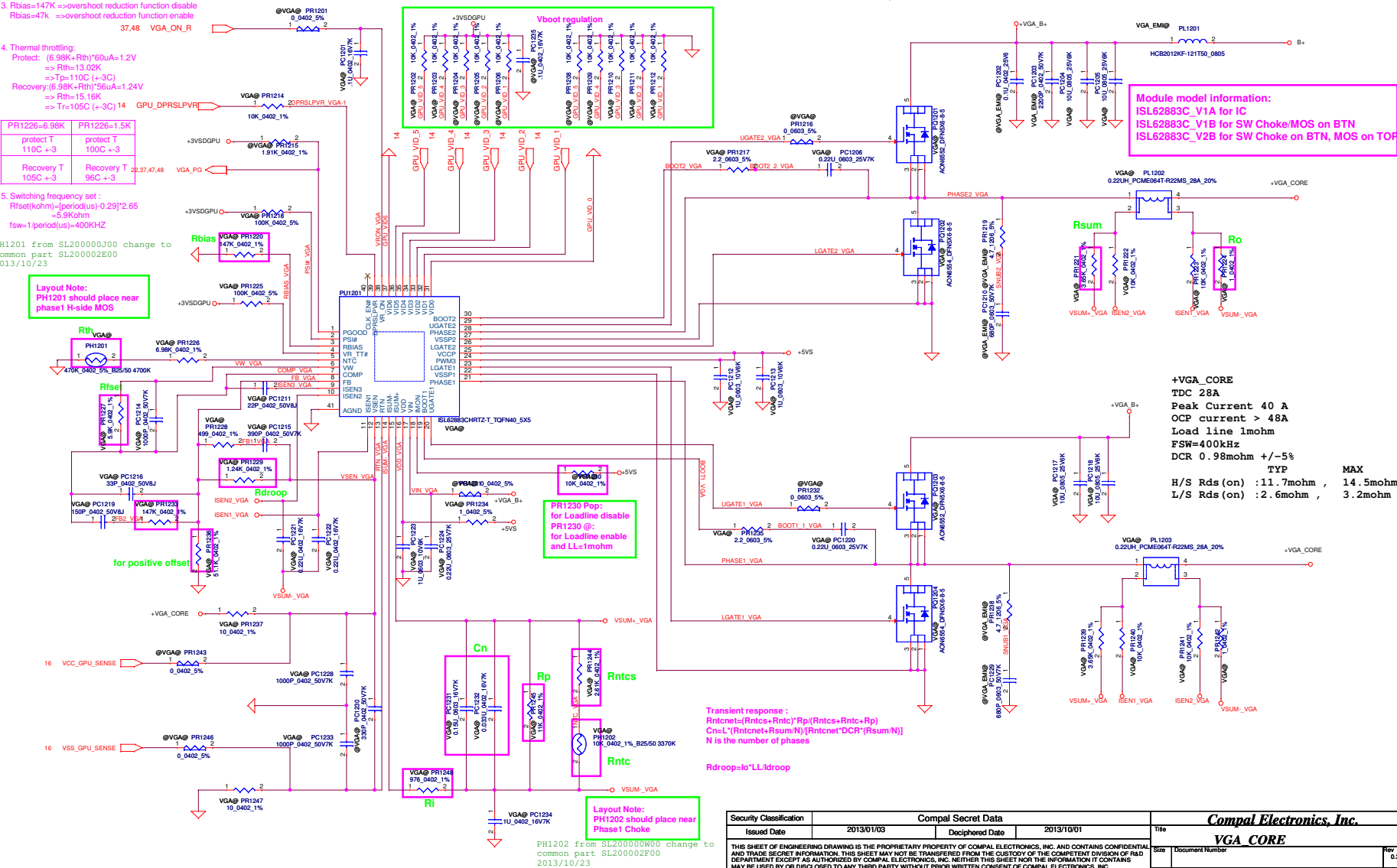
	AMD MARS series				AMD SUN series			Description
	LP: DDR3 ProXT/XTX: GDDR5				UL: DDR3 ProXT/XTX: GDDR5			
GPU	MARS TXX	MARS XT	MARS PRO	MARS LP	SUN UL	SUN PRO	SUN XT	NA
VDDC	0.775-1.175V	0.775-1.125V	0.775-1.050V	0.775-1.000V	0.775-1.125V	0.800-1.075V	0.800-1.150V	NA
TDC	32A (TDC)	25A (TDC)	21A (TDC)	17A (TDC)	16A (TDC)	19A (TDC)	25A (TDC)	NA
EDC	48A	37.5A	31.5A	26A	24A	28.5A	37.5A	NA
OCp	57.6A	45A	37.8A	31.2A	28.8A	34.2A	45A	NA
Vboot	0.85V	0.85V	0.85V	0.85V	0.9V	0.9V	0.9V	NA
Load line	1mohm	1mohm	1mohm	*****	*****	*****	1mohm	NA
Ri PR1248	1.13K Ohm	887 Ohm	750 Ohm	*****	*****	*****	887 Ohm	for OCP and LoadLine Setting
Rdroop PR1229	1.43K Ohm	1.13K Ohm	953 Ohm	*****	*****	*****	1.13K Ohm	for LoadLine Setting
PR1233	187K Ohm	147K Ohm	124K Ohm	*****	*****	*****	147K Ohm	for Compensation
PR1236	51.1K Ohm	51.1K Ohm	51.1K Ohm	*****	*****	*****	51.1K Ohm	for Positive offset

Remark: MARS LP/ SUN UL/ SUN PRO don't use this 2-phase solution

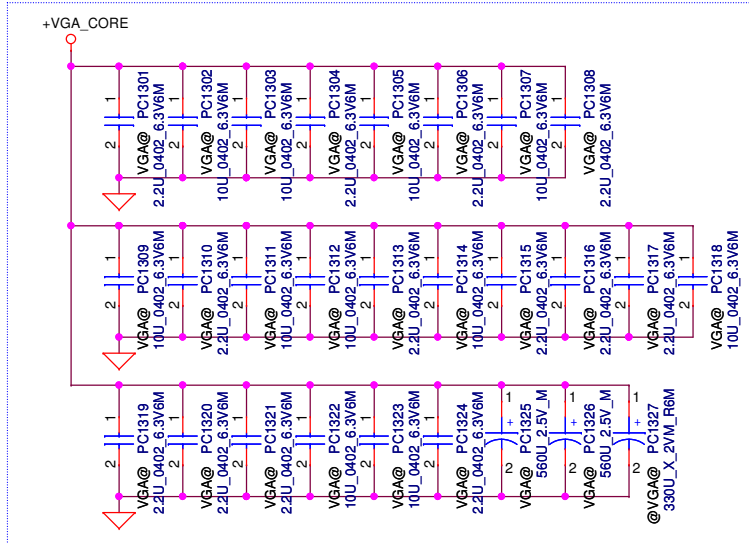
H-side MOS:TPCA8065
Rds(on):
9.4mohm@Vgs=10V
11.7mohm@Vgs=4.5V
Id :16A@Ta=25 degC

L-side MOS:TPCA8057
Rds(on):
2.0mohm@Vgs=10V
2.6~3.2mohm@Vgs=4.5V
Id :42A@Ta=25 degC

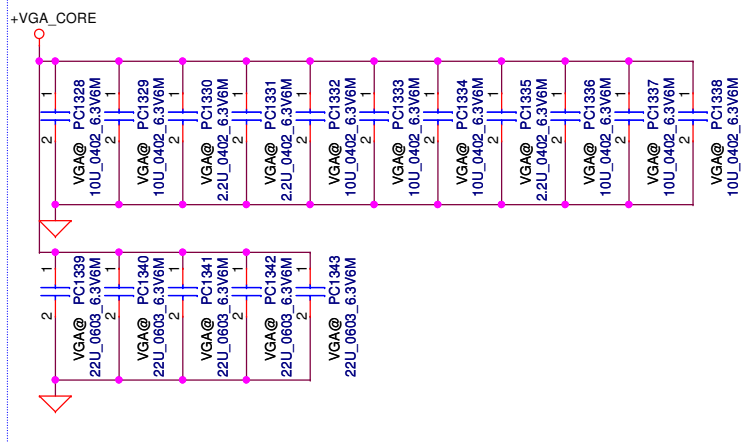
Choke: 0.22uH (Size:7*7*4)
Rdc=0.98mohm +-5%
Heat Rating Current=28A
Saturation Current=28A



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AMD MARS
GPU_CORE
560uF*2+330uF*1
10uF*11+2.2uF*13



AMD MARS
meet ripple
22uF*5+10uF*8+2.2uF*3

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		layout area not enough		APU_CORE	PQ801;PQ803;PQ807;PQ808 FDMS7698 and PQ802;PQ804;PQ806;PQ809 MDU1511 change to Dual N AON6932A	10/09	EVT
2		EMI bead "HCB2012KF-121T50_0805" derating 5A, need 2pcs for APU_CORE and APU_CORENB		APU_CORE	Add PL806 EMI bead "HCB2012KF-121T50_0805" from 1pcs to 2pcs at B+, for APU_CORE and APU_CORENB	10/15	EVT
3		RT8880A FAE review		APU_CORE	PR813 from 0402 change to 0603, delete PR844, PR847	10/16	EVT
4		HW: EC share ROM, modify 3VALW and 1.1VALW enable net-name		3VALW 5VALW	change 3VALW enable net name from 3V5V_EN to 3V_EN change 1.1VALW enable net name from SUSP# to 1.1V_EN	10/17	EVT
5		Choke, OS-CON cap, Thermistor change to standard part				10/23	EVT
6		RT8880A vendor EOL, change to RT8880B		APU_CORE	CPU_CORE IC from RT8880A SA000066V00 change to RT8880B SA000066V10	10/23	EVT
7		Battery connector BATT+ bead, 1pcs for UMA, 2pcs for DIS.		BATT CONN	Add PL202 HCB2012KF-121T50_0805 for DIS only	10/28	EVT
8		22U_0603_6.3V6M cheaper than 47U_0603_6.3V6M		+1.05VS +1.1VALW	PC609, PC610 and PC709, PC710 from 47U_0603_6.3V6M change to 22U_0603_6.3V6M	10/30	EVT
9		HW request Add PR1107, and unpop PR1104, VGA_PG is default setting for VGA sequence control		+0.95V	Add location PR1107 0_0402_5%, and unpop PR1104 0_0402_5%	10/31	EVT
10		HW request add RC at 3VALW enable		+3VALW	Add PR413 0_0402_5%, and PC428 0.1U_0402_10V7K _ un-pop	10/31	EVT
11		adjust 1.05V output voltage		+1.05VSP	change PR607 from 100K ohm to 15.4K ohm, change PR609 from 133K ohm to 20K ohm, change 1.05V output from 1.05V to 1.062V	12/02	DVT
12		adjust 1.8VSP output voltage		+1.8VSP	change PR723 from 20K ohm to 20.5K ohm, change 1.05V output from 1.8V to 1.83V	12/10	DVT
13		adjust 1.1VALW output voltage		+1.1VALW	change PR709 from 118K ohm to 115K ohm, change 1.1VALW output from 1.108V to 1.121V	12/10	DVT
14		Part count reduce			change enable resistor PR413, PR602, PR702, PR724 from 0 ohm to R-Short, change EMI High side and Low side resistor PR308, PR407, PR605, PR705, PR801, PR820, PR849, PR860, PR1216, PR1232 from 0 ohm to R-Short.	12/10	DVT
15		adjust VGA Vboot voltage		VGA	change PR1205 from pop to un-pop, change PR1211 from un-pop to pop.	12/13	DVT
16		reserve PD801		CPU_CORE	reserve PD801 for AMD CPU leakage voltage from APU_SVD	12/13	DVT
17		delete VCIN0 and VCIN1 hysteresis		OTP	change PR216 from 22.6K to 16K, change PR227 from 26.1K to un-pop, change PR202 from UMA/10.5K and DIS/11.3K to 10K, change PR223 from UMA/162K and DIS/100K to un-pop.	12/24	DVT
18		ABO request BI pin short to GND		BATT CONN	change PR210 from 1k to 0 ohm.	12/26	DVT MEMO
19		65W and 40W VCIN0 set at the same voltage active and recovery		OTP	change UMA SKU PR203 from 10K to 44.2K Add PC426	12/26	DVT MEMO

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3					
4					

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